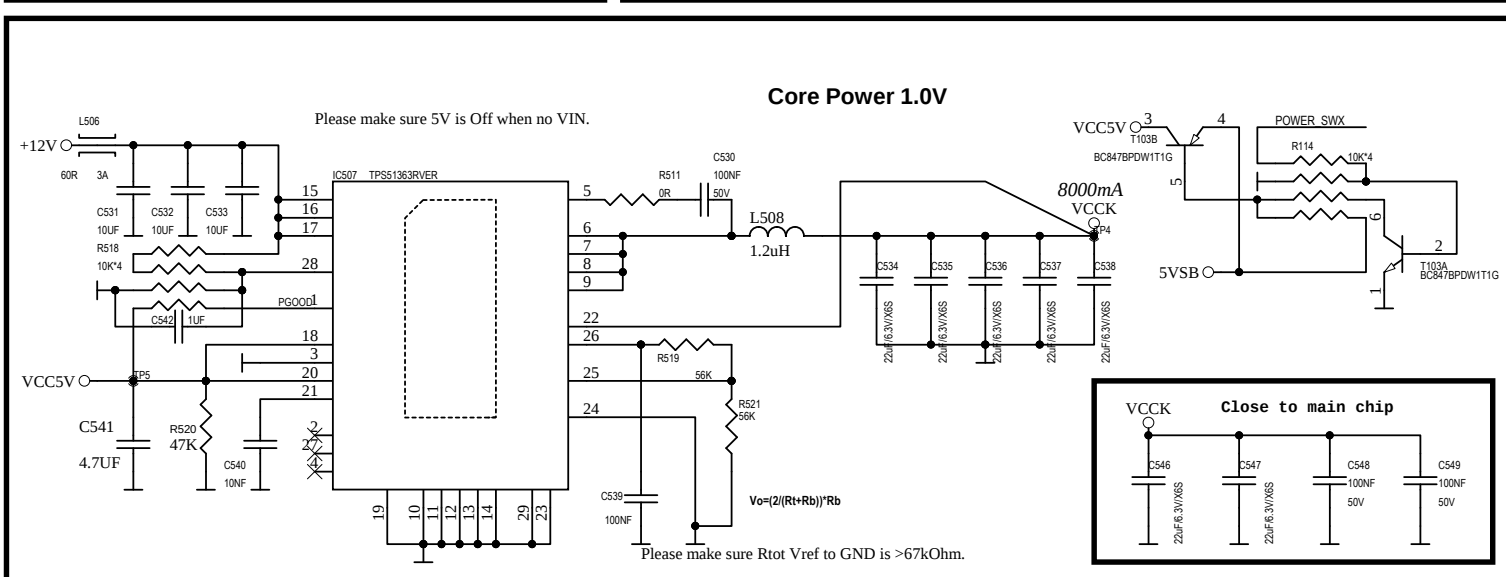


[illegible][illegible]

USB / MHL Power

The schematic diagram illustrates the USB/MHL Power section of the TP565286RHDR IC. The IC is shown with its pin connections and internal components. Key components and connections include:

- Input/Output Capacitors:** C560, C561, C562 (10uF) are connected to the +24V_AU input. C565 (1uF) and C567 (100nF) are connected to the DVDD3V3 input. C551 (100pF) and C568 (82pF) are connected to the +5V_SW output.
- Inductor:** L511 (6.8uH) is connected in the power path between the input and output.
- Feedback Network:** Resistors R527 (100k), R532 (10k), R533 (10k), R534 (39k), R535 (10k), R540 (2.7k), R541 (2.7k), R543 (100R), R544 (100R), and R546 (100R) are connected to various internal nodes and the output.
- Compensation Capacitors:** C555 (47nF), C563 (100nF), and C564 (82pF) are connected to internal nodes.
- Internal Nodes:** The IC has several internal nodes labeled: EPAD, AGND, RSET2, RSET1, RLIM, COMP, FB, SS, LX, BST, SW_IN2, SW_IN1, nFAULT1, nFAULT2, EN, SW_OUT2, SW_OUT1, SW_EN2, SW_EN1.
- Legend:** Hi: ON, Lo: OFF.

MAIN POWER CONNECTOR

Diagram showing the main power connector pinout and connections:

- Pin 16:** GND
- Pin 15:** GND
- Pin 1:** SS00
- Pin 2:** TP8
- Pin 3:** C552 (100UF)
- Pin 4:** TP8
- Pin 5:** C553 (100NF)
- Pin 6:** C554 (100NF)
- Pin 7:** C555 (100NF)
- Pin 8:** TP12
- Pin 9:** +24V_AU
- Pin 10:** POWER_SWX
- Pin 11:** P14 R549 (OR LD CK)
- Pin 12:** P16 R550 (OR LD DI)
- Pin 13:** BRIGHT_ADJ
- Pin 14:** INVERTER_ON_OFF

Additional components and connections:

- TP8:** 5VSB
- TP12:** +24V_AU
- C555:** 100NF
- C556:** 100NF

Local Dimming
Place close to R3431 and R3443.

[illegible][illegible]

Tuner Power

IC500
XC8107AC05MR-GW

AVDD3V3

+3V3_TUNER

5 VIN VOUT 1

4 CE VSS FLG 3

C501 1uF

C502 1uF

Imax=300mA

R551 22K

AVDD3V3

eMMC 1V8

The schematic shows the power supply for the eMMC. A 1.8V regulator (TP10) is connected to LDO_PWR. The output of the regulator is connected to the VIN pin of the eMMC chip (IC501) through a 1K resistor (R500). A 1uF capacitor (C500) is connected between the VIN pin and ground. The eMMC chip's CE, VSS, and VOUT pins are connected to ground. The eMMC chip is also connected to the LDO_PWR line through a 22uF capacitor (C506).

[illegible]

BRIGHT ADJUST

LD CE

R525

OR

3V3SB

5

4

TP18

BRIGHT_ADJ

R542 100R

NC

1

2

3

R539 OR

BL DIMMING

NL17S232DFT2G

BRIGHT_ADJ
Normal = > Max:3V3, Min:0V
Stand_By = > 0V

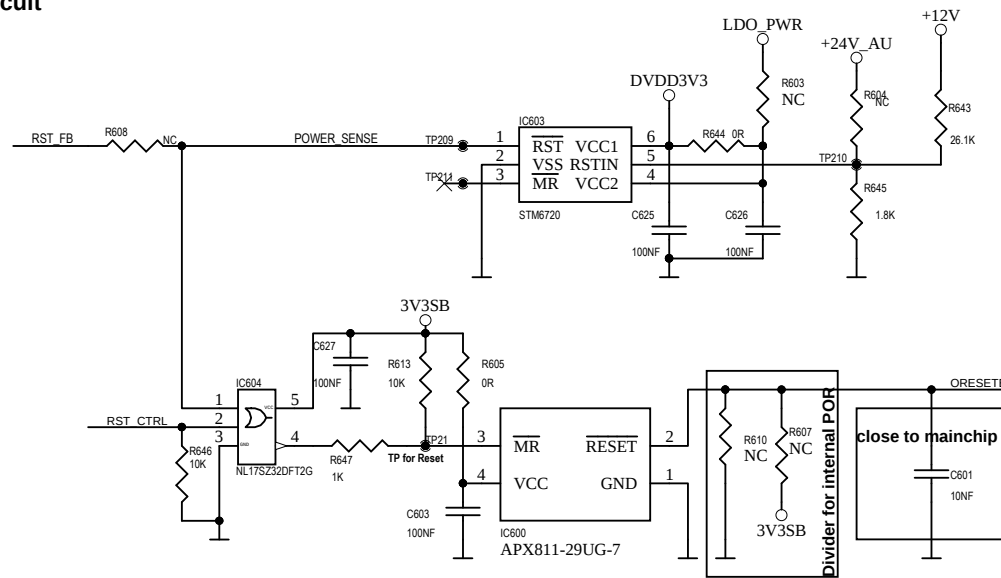
Demod PWR

[illegible][illegible]

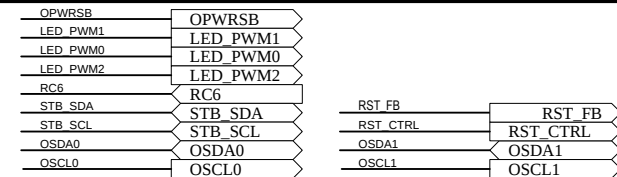
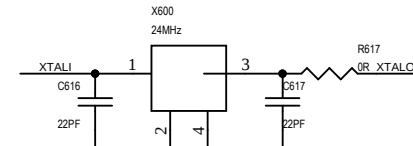
BL_ON/OFF	BL_ON/OFF
BL_DIMMING	BL_DIMMING
OPWRSB	OPWRSB
POWER_OK	POWER_OK
PANEL_VCC_ON/OFF	PANEL_VCC_ON/OFF
USB2_PWEN	USB2_PWEN
USB1_PWEN	USB1_PWEN
DDR_PWR_EN	DDR_PWR_EN
SP1_CK	SP1_CK
SP1_DI	SP1_DI
SP1_DO	SP1_DO
SP1_CE	SP1_CE

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Size A4	Number ZAT190R-1			Revision V-2	
Date:	24.02.2016			Sheet of	
File:	\\.\05_System Power.SchDoc			Drawn By:Osman OSMAN	

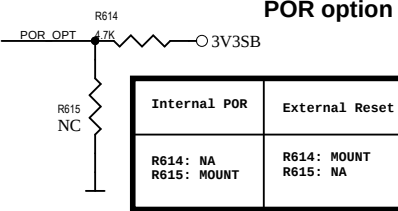
Reset circuit



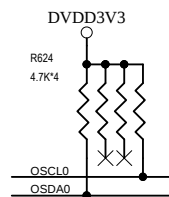
CRYSTAL(24MHz)



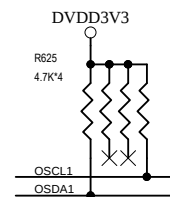
POR option



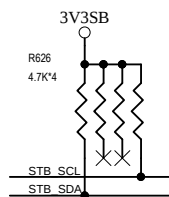
1st I2C



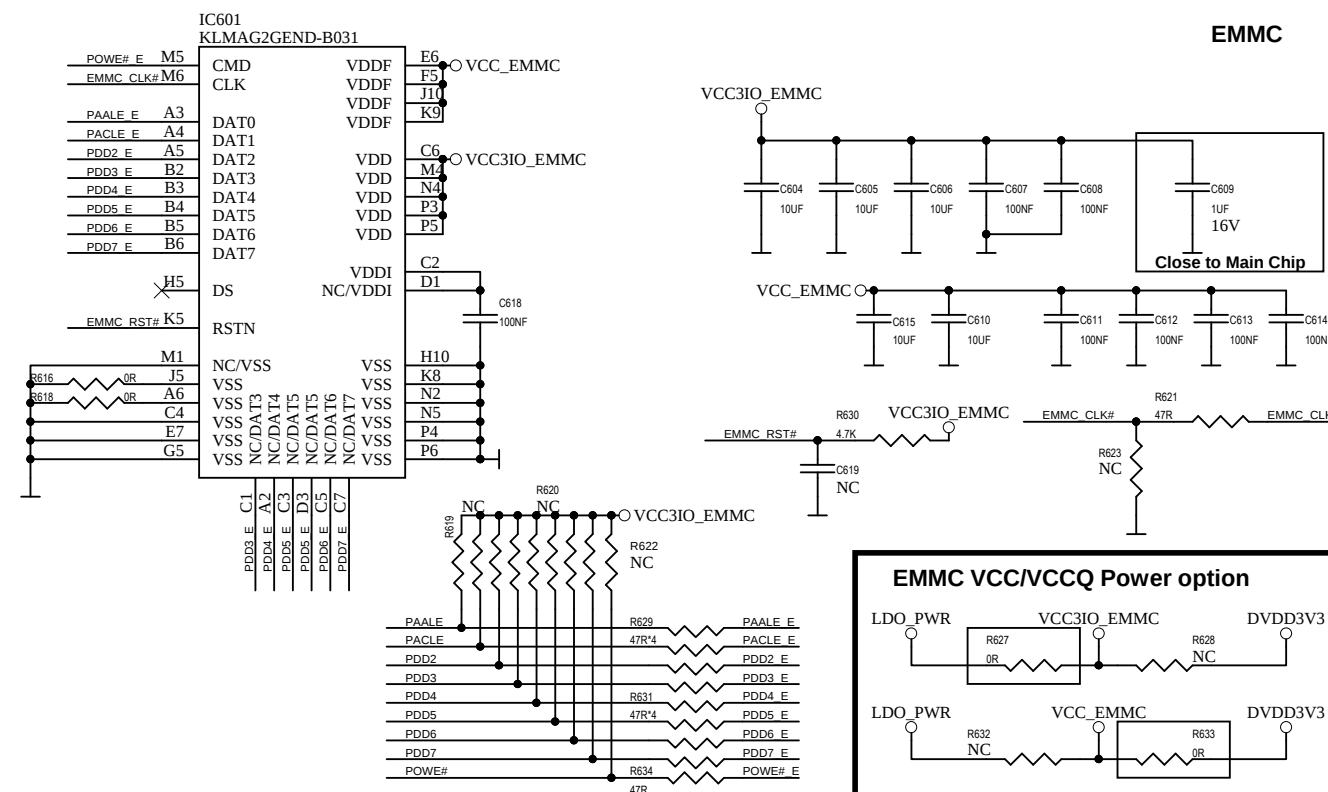
2nd I2C



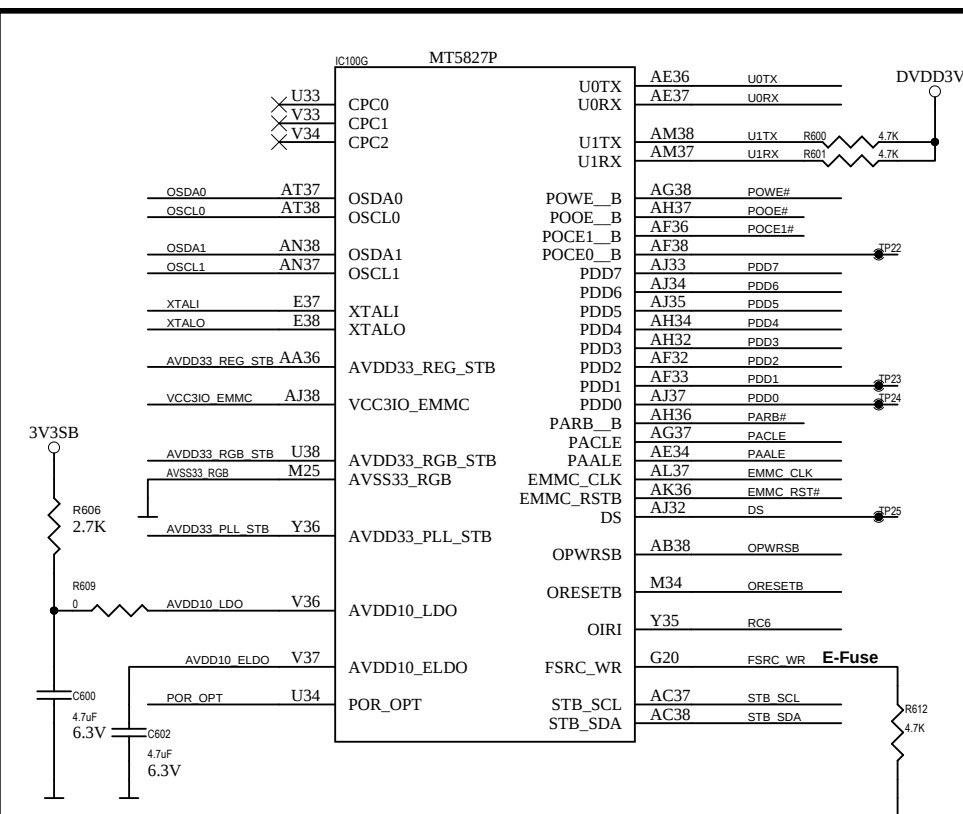
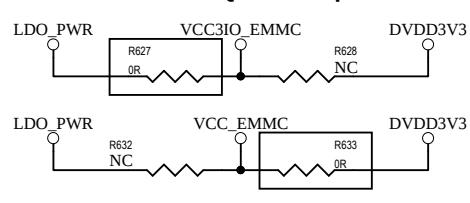
3rd I2C



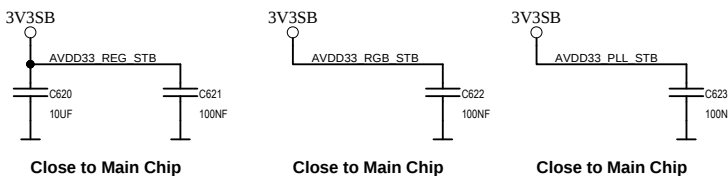
EMMC



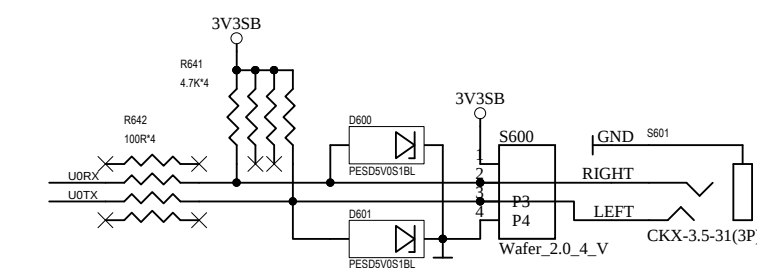
EMMC VCC/VCCQ Power option



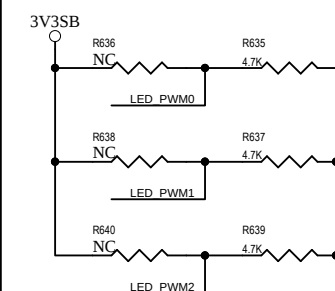
Analog Power



UART connector for code download and debug

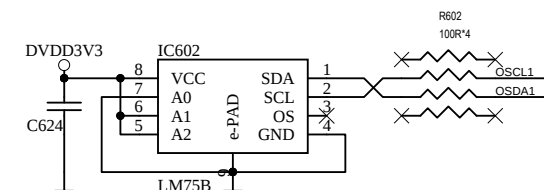


STRAPPING



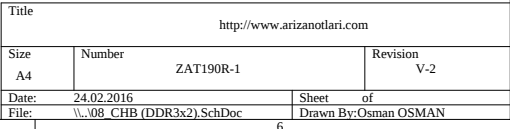
STRAPPING	LED_PWM0	LED_PWM1	LED_PWM2
ICE mode + 24M + ROM to eMMC boot from eMMC pins (share pins w/s NAND)	0	0	0
ICE mode + 24M + serial boot	0	0	1
ICE mode + 24M + ROM to 60bit ECC Nand boot	0	1	0
ICE mode + 24M + serial boot(with GPIO)	0	1	1

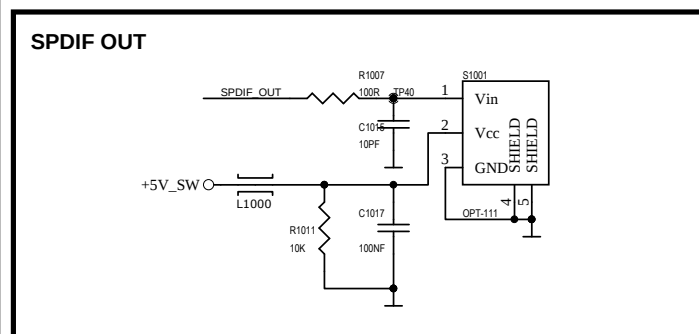
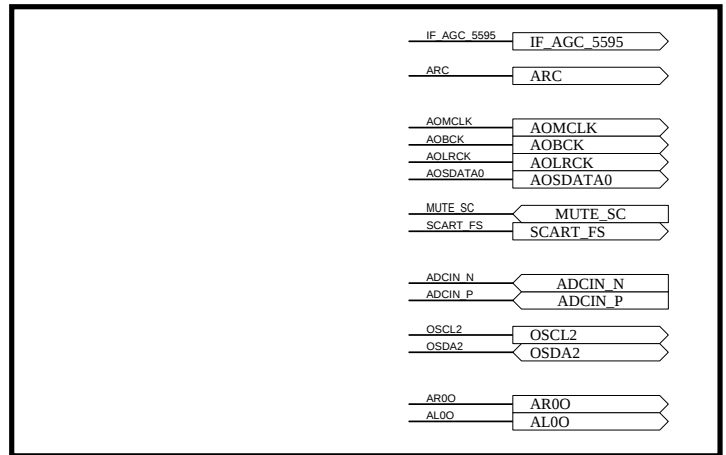
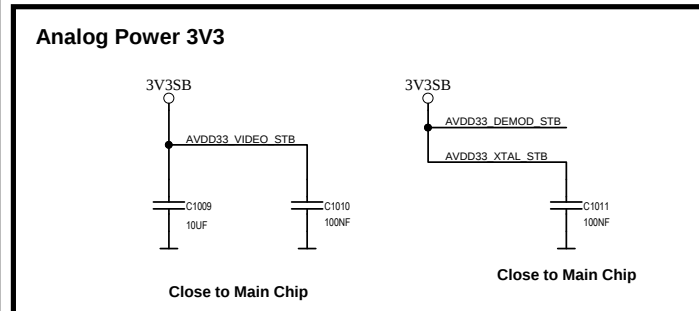
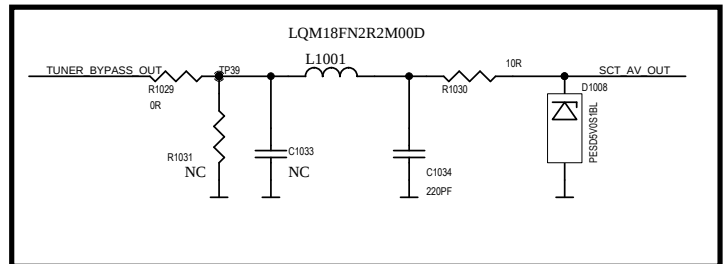
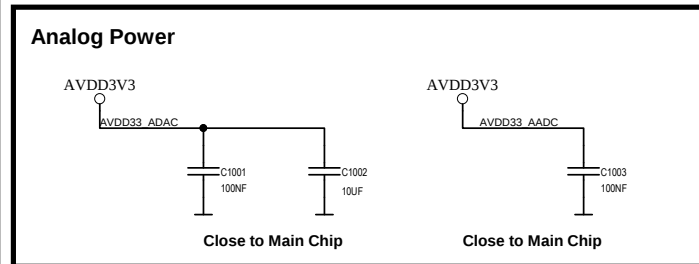
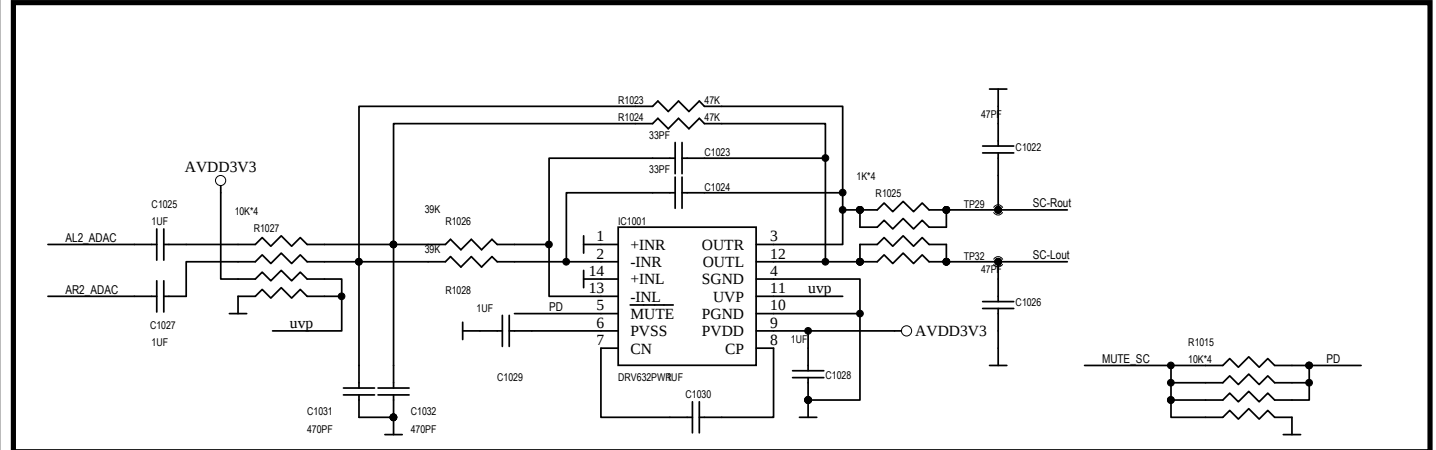
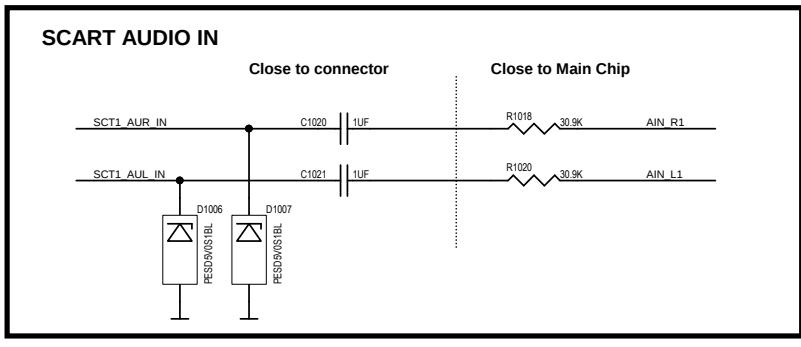
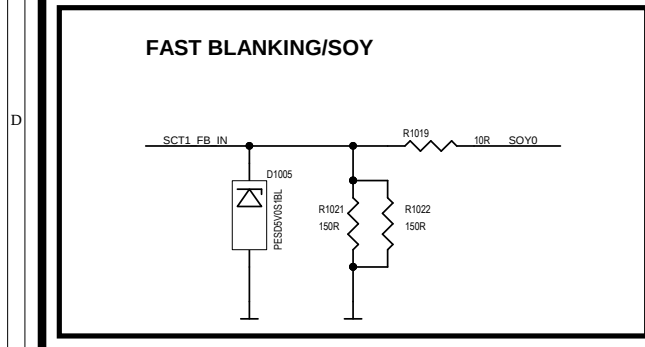
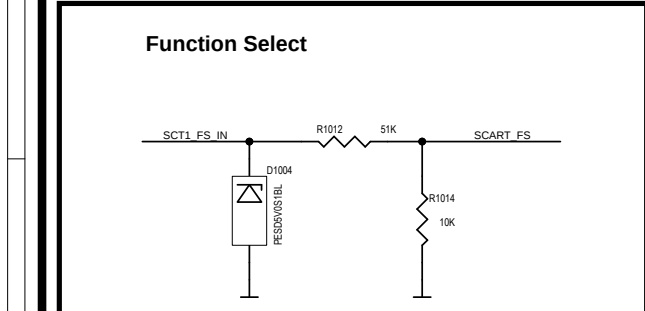
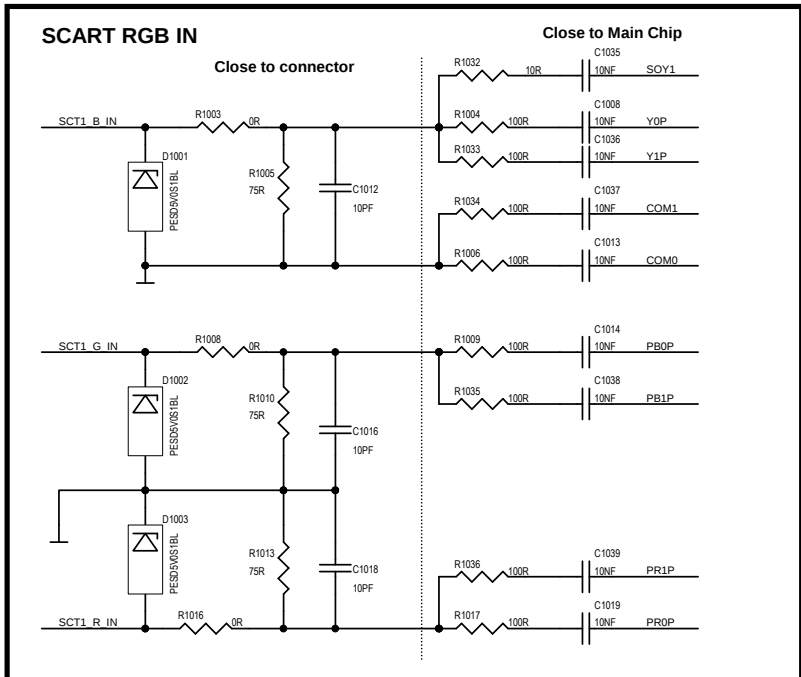
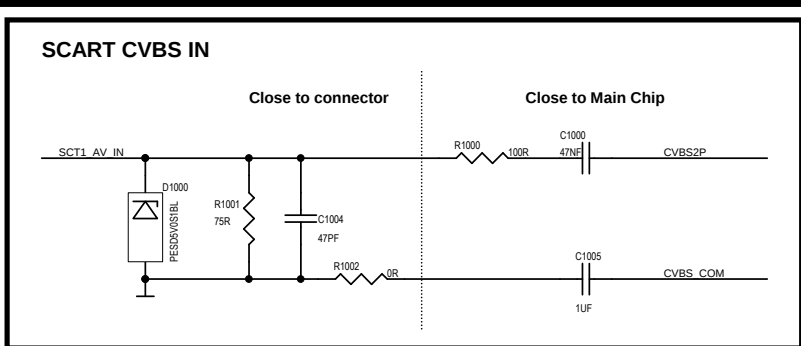
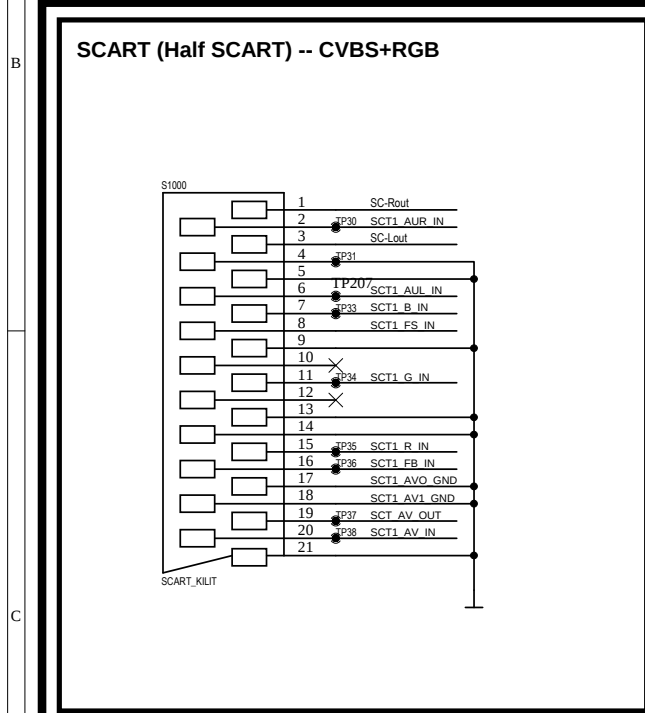
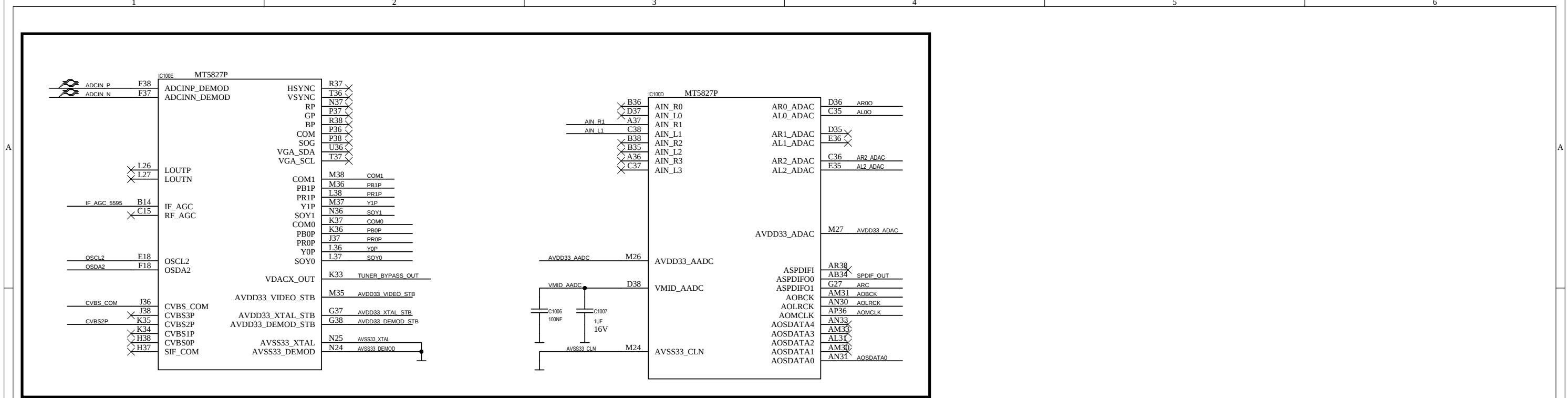
Thermal sensor



Place it on top side (most cool place).

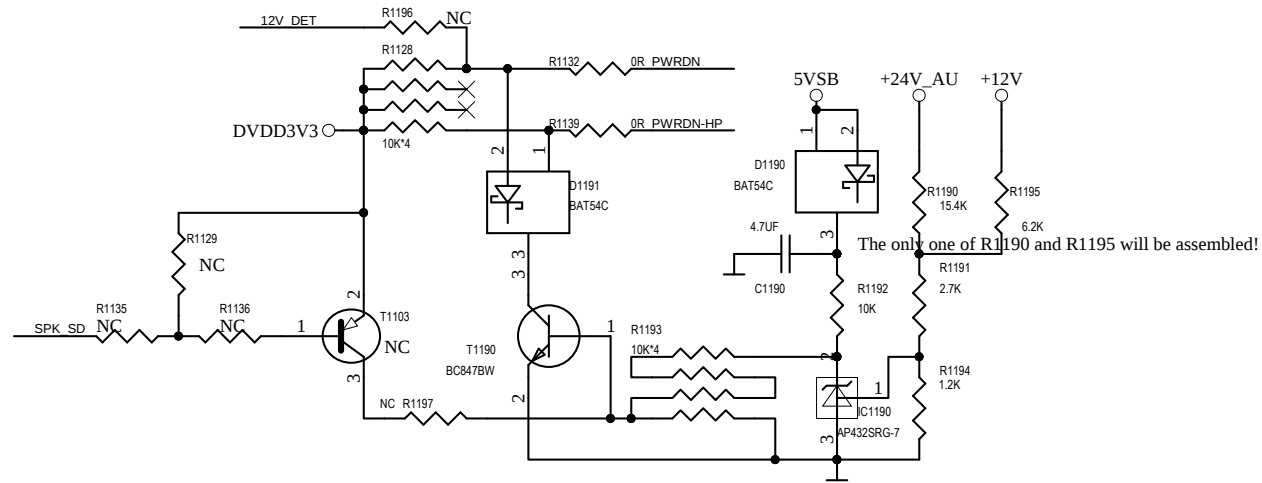
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Size	Number	ZAT190R-1	Revision
A4			V-2
Date:	24.02.2016	Sheet	of
File:	\\..06_Peripheral.SchDoc	Drawn By:	Osman OSMAN
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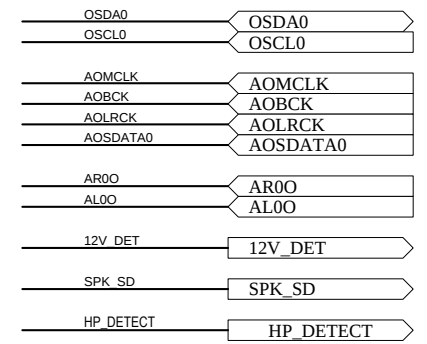
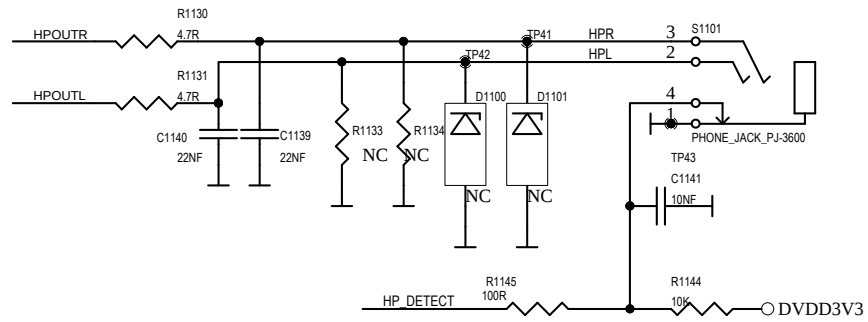


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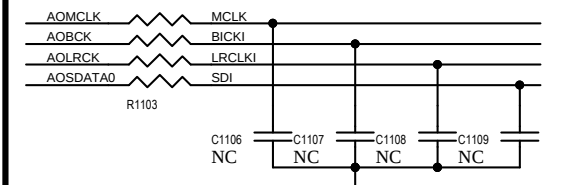
ANTI-POP CIRCUIT



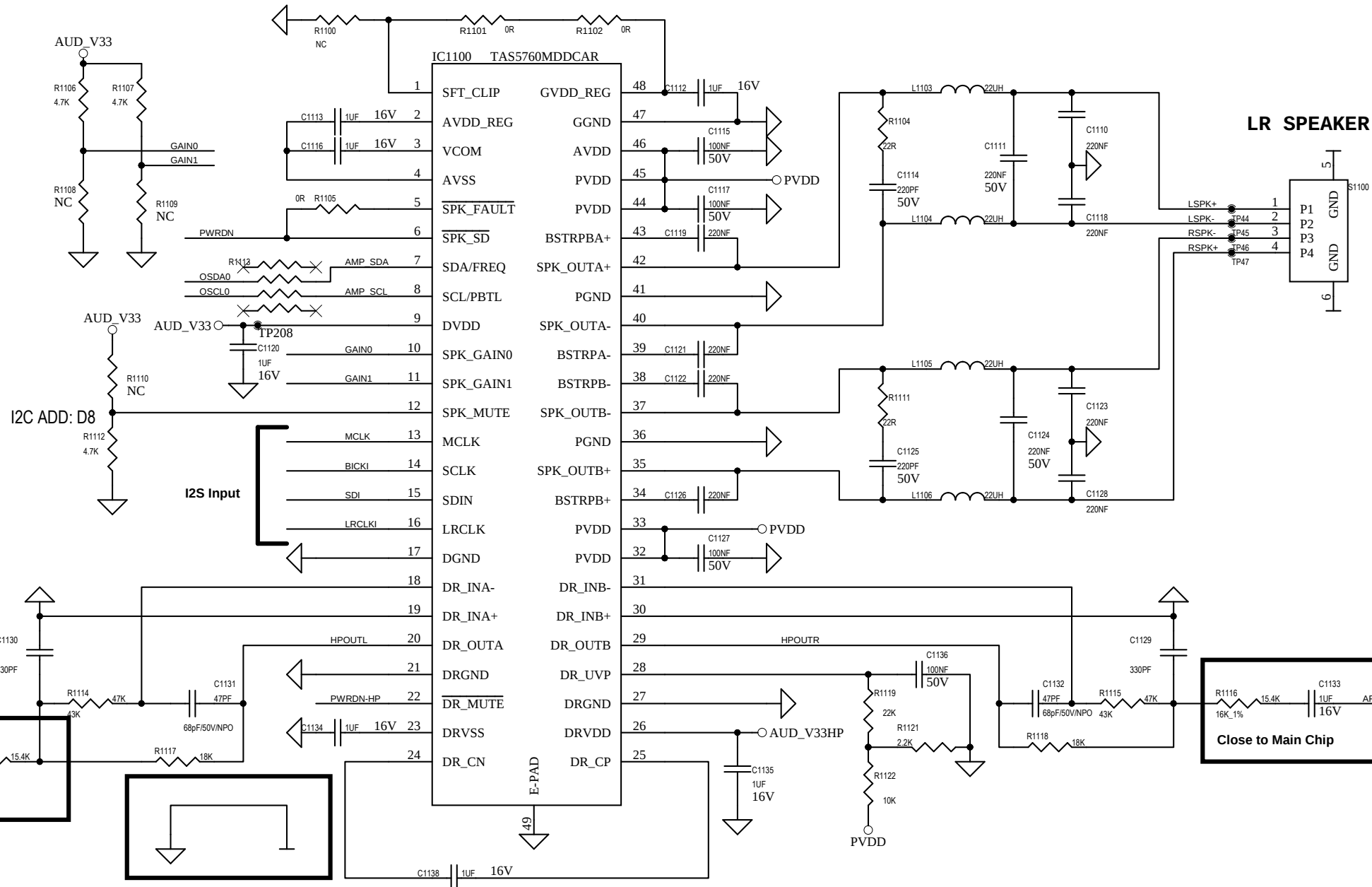
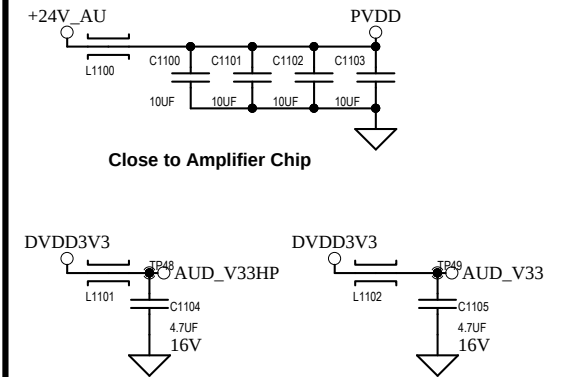
HEADPHONE CONNECTOR



EMI/Crosstalk reduction



AUDIO POWER

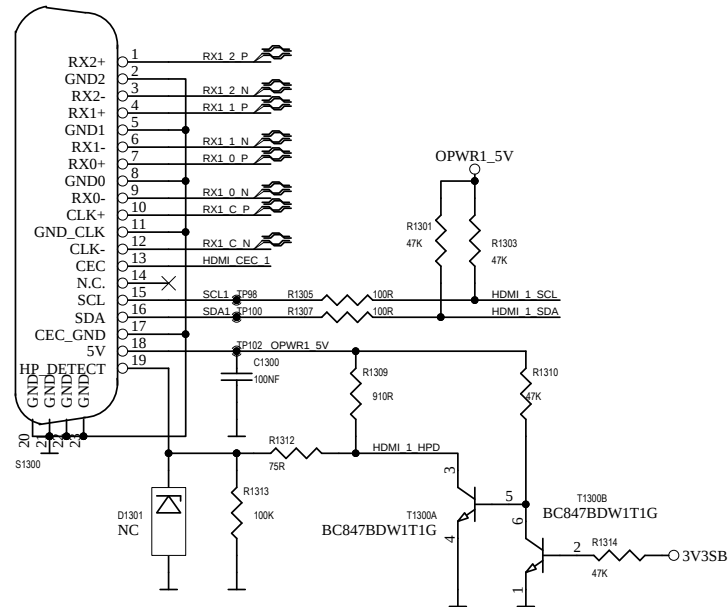


Close to Main Chip

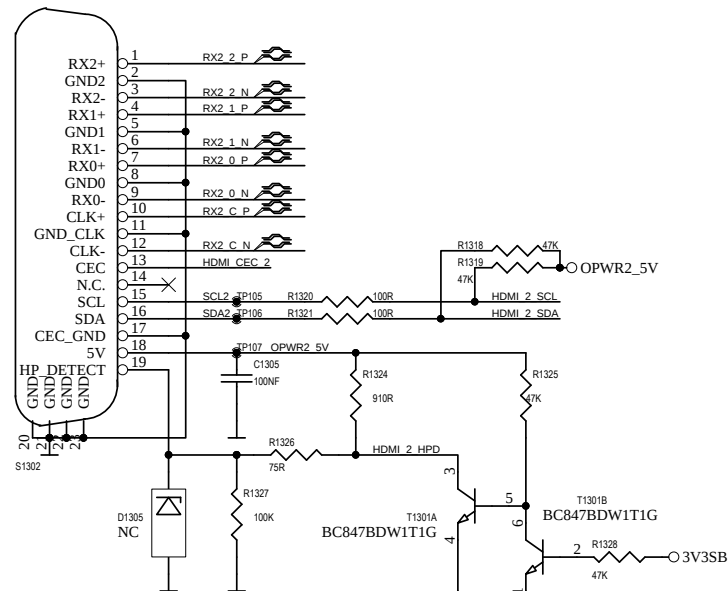
Close to Main Chip

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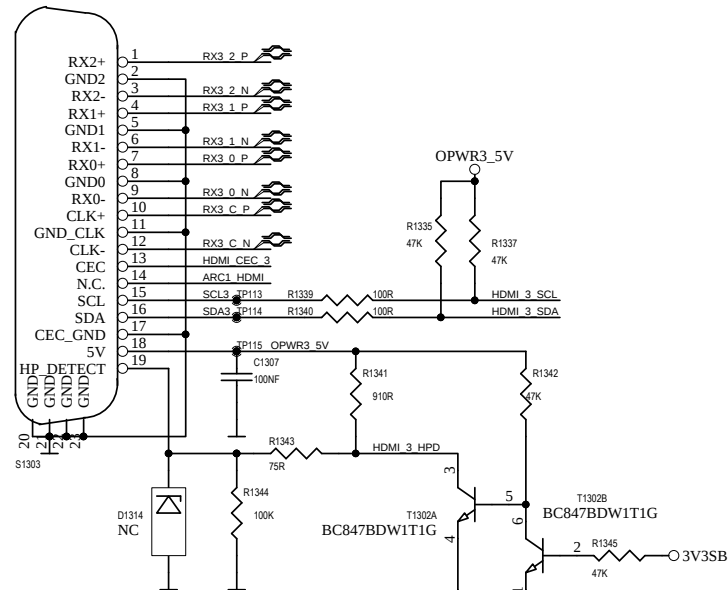
HDMI Port 1 (Embedded EDID)



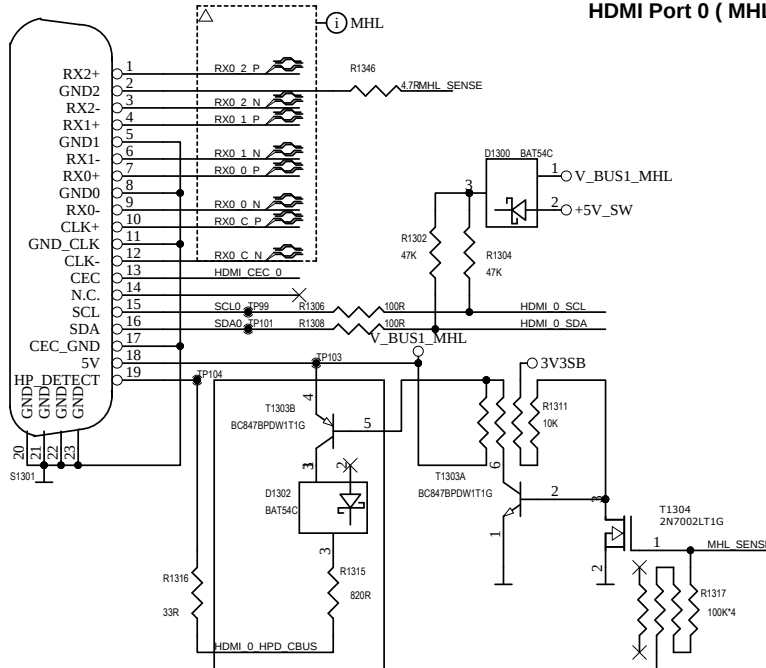
HDMI Port 2 (Embedded EDID)



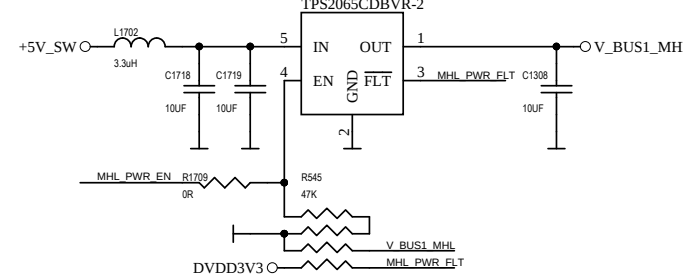
HDMI Port 3 (Embedded EDID)



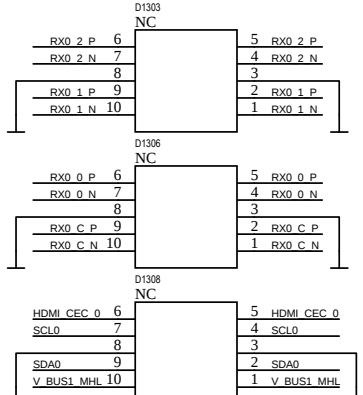
HDMI Port 0 (MHL)



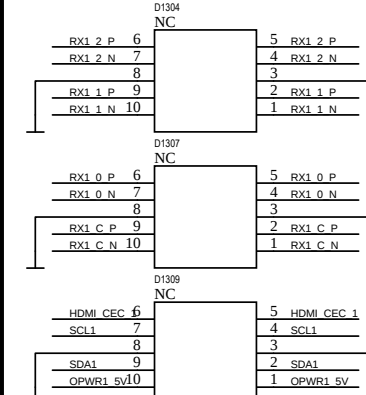
HDMI Port 0 (MHL) POWER



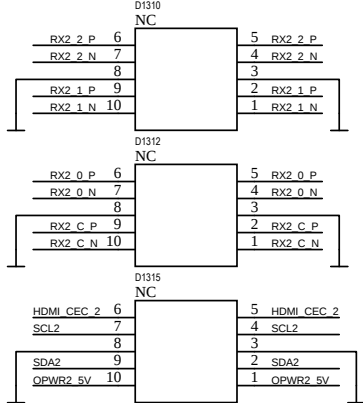
HDMI Port 0 (MHL) PROTECTION



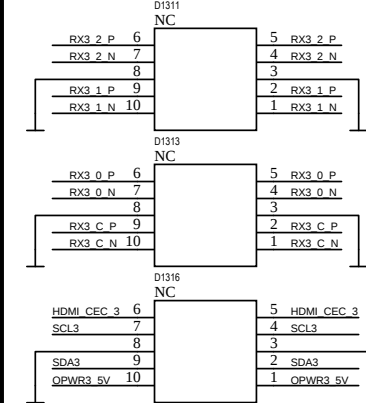
HDMI Port 1 PROTECTION



HDMI Port 2 PROTECTION



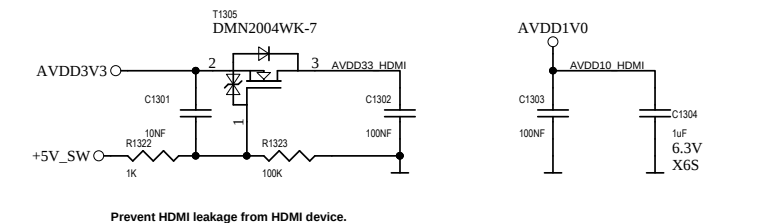
HDMI Port 3 PROTECTION



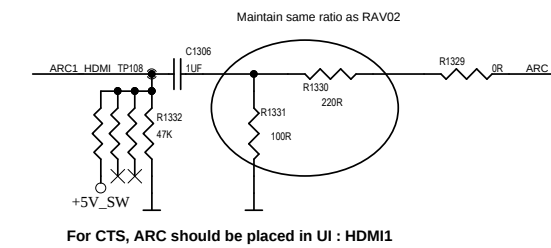
SoC HDMI Block

CEC		IC100F	MT5827P		
	G24	HDMI_CEC		A20	R137A 4.7R RX0 0 P
			HDMI_0_RX_0	B20	R137A 4.7R RX0 0 N
HDMI 0_SCL	F26	HDMI_0_SCL	HDMI_0_RX_0B	A19	R137A 4.7R RX0 1 P
HDMI 1_SCL	G30	HDMI_1_SCL	HDMI_0_RX_1	B19	R137A 4.7R RX0 1 N
HDMI 2_SCL	G31	HDMI_2_SCL	HDMI_0_RX_1B	A18	R137A 4.7R RX0 2 P
HDMI 3_SCL	D34	HDMI_3_SCL	HDMI_0_RX_2	B18	R137A 4.7R RX0 2 N
			HDMI_0_RX_2B	A21	R137A 4.7R RX0 C P
HDMI 0_SDA	F27	HDMI_0_SDA	HDMI_0_RX_C	B21	R137A 4.7R RX0 C N
HDMI 1_SDA	G28	HDMI_1_SDA			
HDMI 2_SDA	F33	HDMI_2_SDA	HDMI_1_RX_0	C23	R137A 4.7R RX1 0 P
HDMI 3_SDA	D33	HDMI_3_SDA	HDMI_1_RX_0B	D23	R137A 4.7R RX1 0 N
			HDMI_1_RX_1	C22	R137A 4.7R RX1 1 P
	✕ G26	HDMI_0_PWR5V	HDMI_1_RX_1B	D22	R137A 4.7R RX1 1 N
HDMI 1_PWR5V	E30	HDMI_1_PWR5V	HDMI_1_RX_2	A22	R137A 4.7R RX1 2 P
HDMI 2_PWR5V	E31	HDMI_2_PWR5V	HDMI_1_RX_2B	B22	R137A 4.7R RX1 2 N
	✕ E34	HDMI_3_PWR5V	HDMI_1_RX_C	A24	R137A 4.7R RX1 C P
			HDMI_1_RX_CB	B24	R137A 4.7R RX1 C N
HDMI 0_HPD_CBUS	F28	HDMI_0_HPD_CBUS			
HDMI 1_HPD	F30	HDMI_1_HPD	HDMI_2_RX_0	A26	R137A 4.7R RX2 0 P
HDMI 2_HPD	F31	HDMI_2_HPD	HDMI_2_RX_0B	B26	R137A 4.7R RX2 0 N
HDMI 3_HPD	F34	HDMI_3_HPD	HDMI_2_RX_1	C25	R137A 4.7R RX2 1 P
			HDMI_2_RX_1B	D25	R137A 4.7R RX2 1 N
MHL_SENSE	F24	MHL_SENSE	HDMI_2_RX_2	C24	R137A 4.7R RX2 2 P
			HDMI_2_RX_2B	D24	R137A 4.7R RX2 2 N
AVDD10_HDMI	B30	AVDD10_HDMI	HDMI_2_RX_C	C26	R137A 4.7R RX2 C P
AVDD10_HDMI	A30	AVDD10_HDMI	HDMI_2_RX_CB	D26	R137A 4.7R RX2 C N
AVDD33_HDMI	P27	AVDD33_HDMI			
AVDD33_HDMI	P28	AVDD33_HDMI	HDMI_3_RX_0	C28	R137A 4.7R RX3 0 P
			HDMI_3_RX_0B	D28	R137A 4.7R RX3 0 N
				D28	

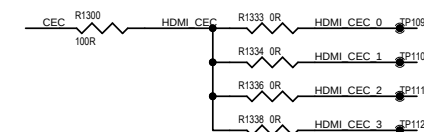
Analog Power



Audio Return Channel (ARC)



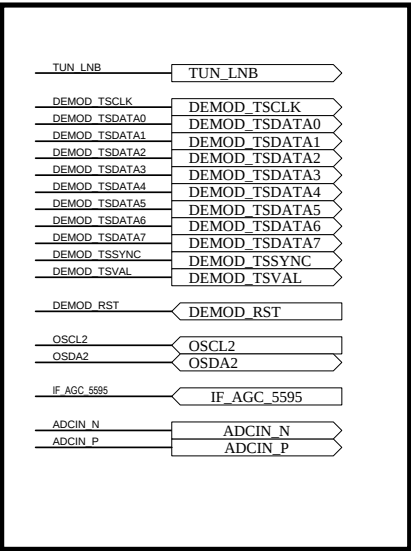
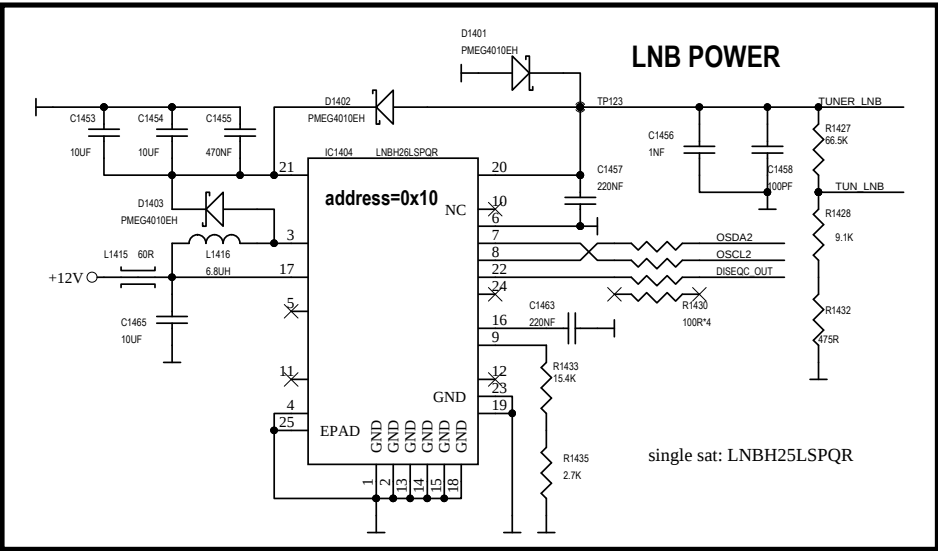
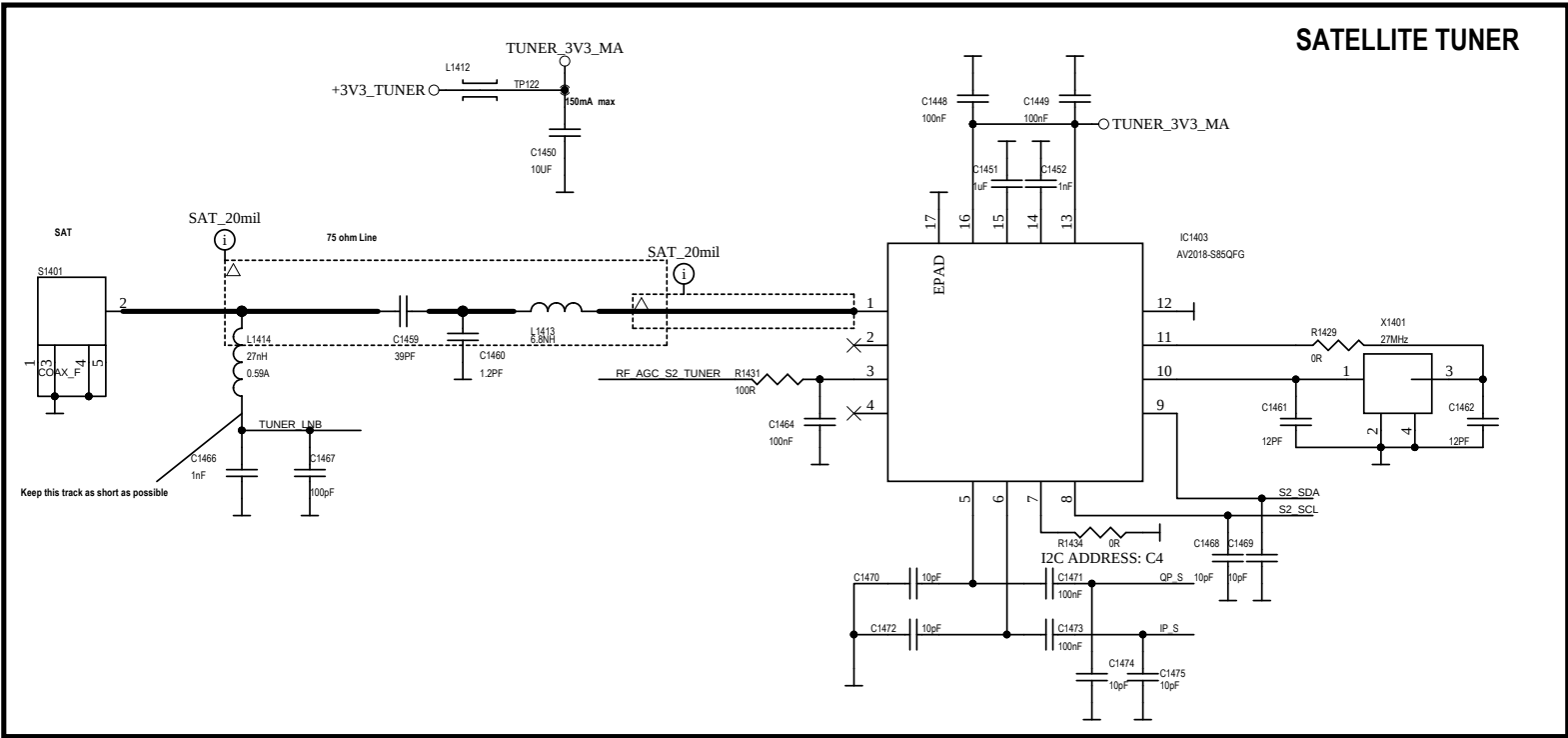
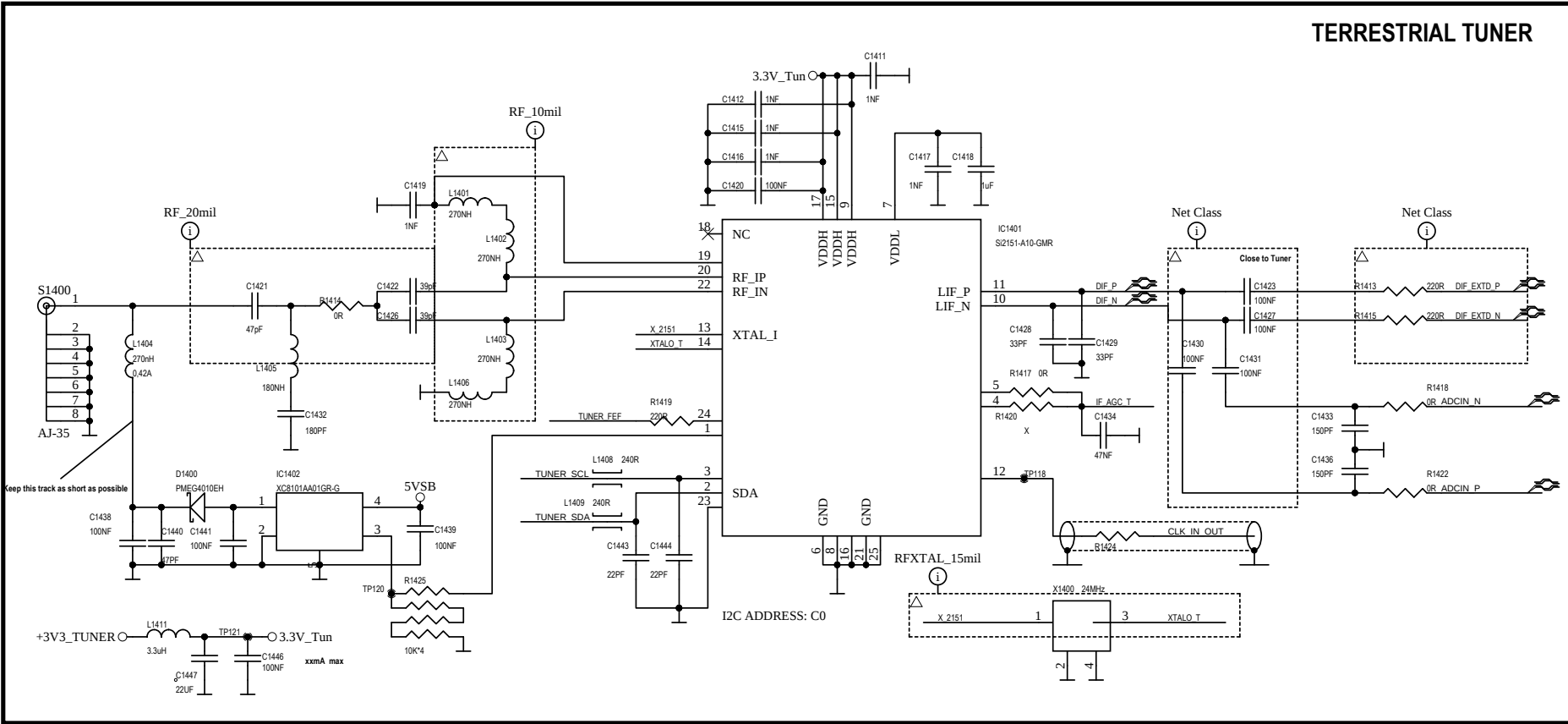
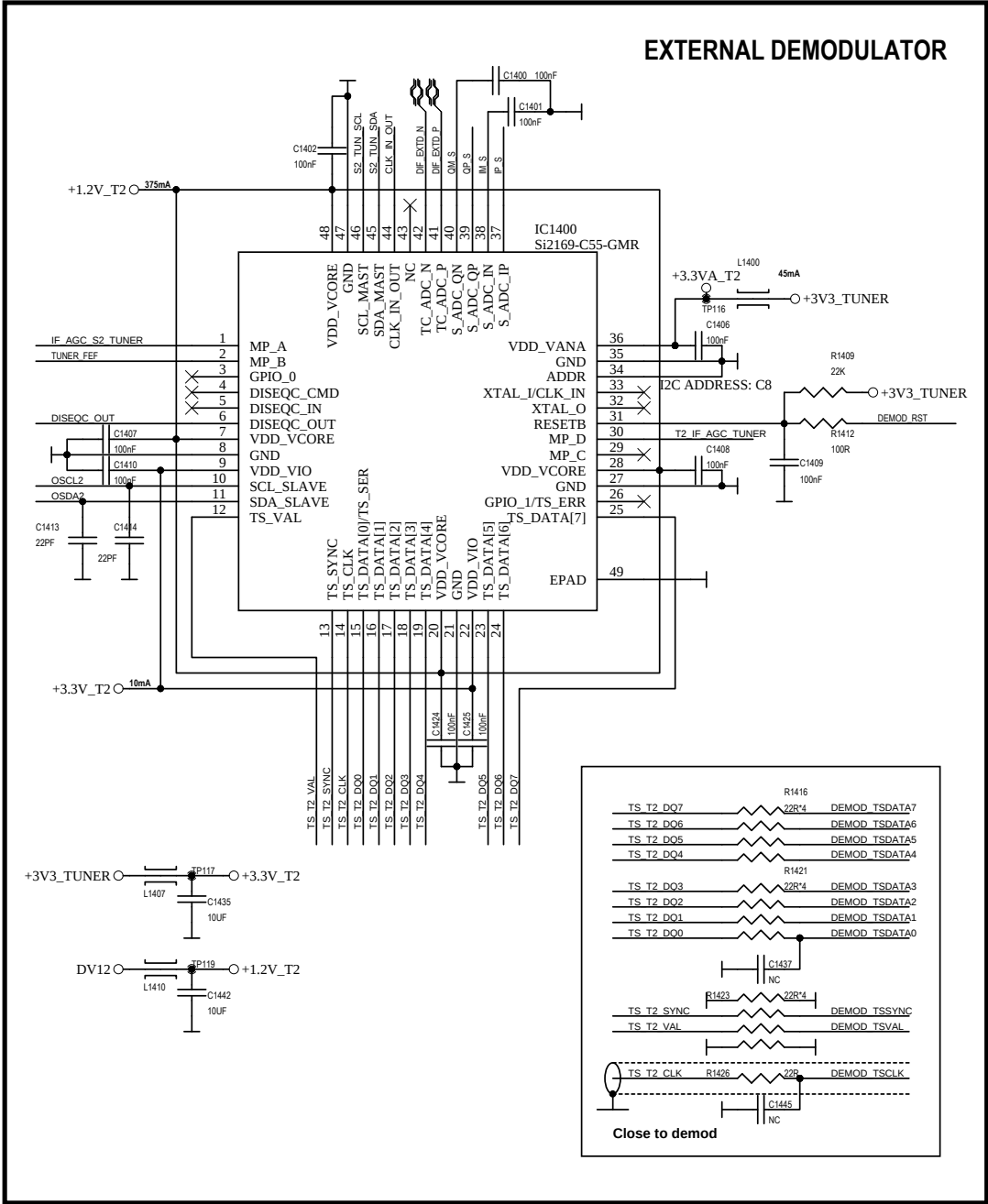
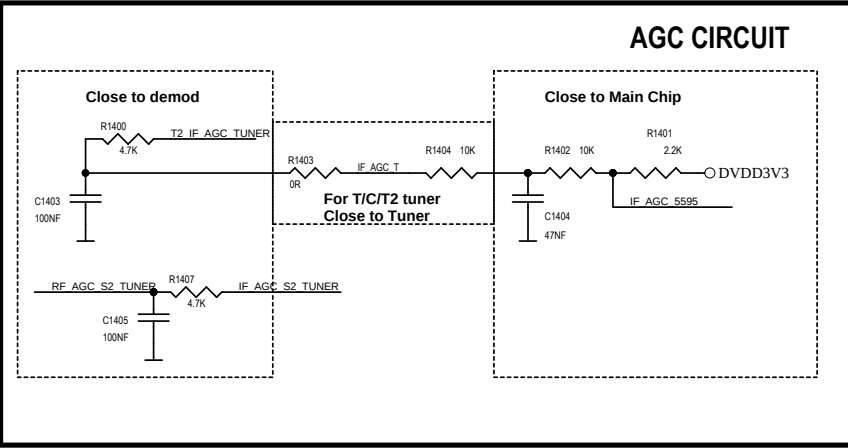
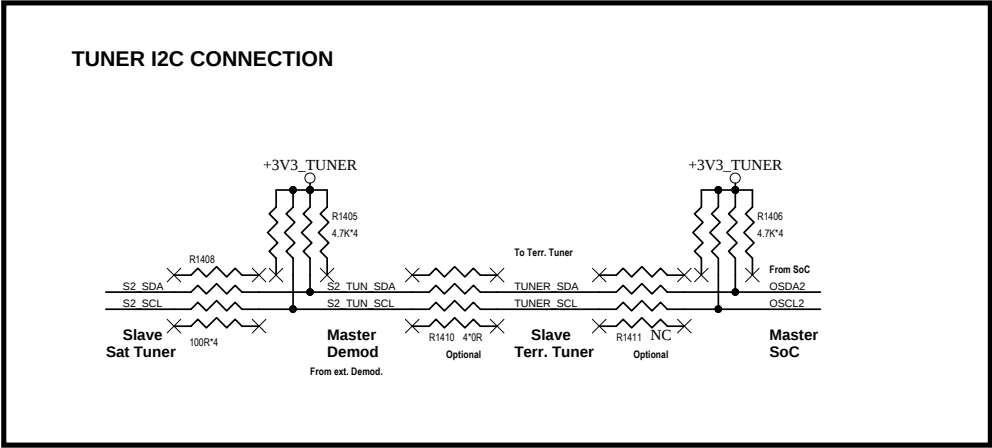
CEC



PORTS

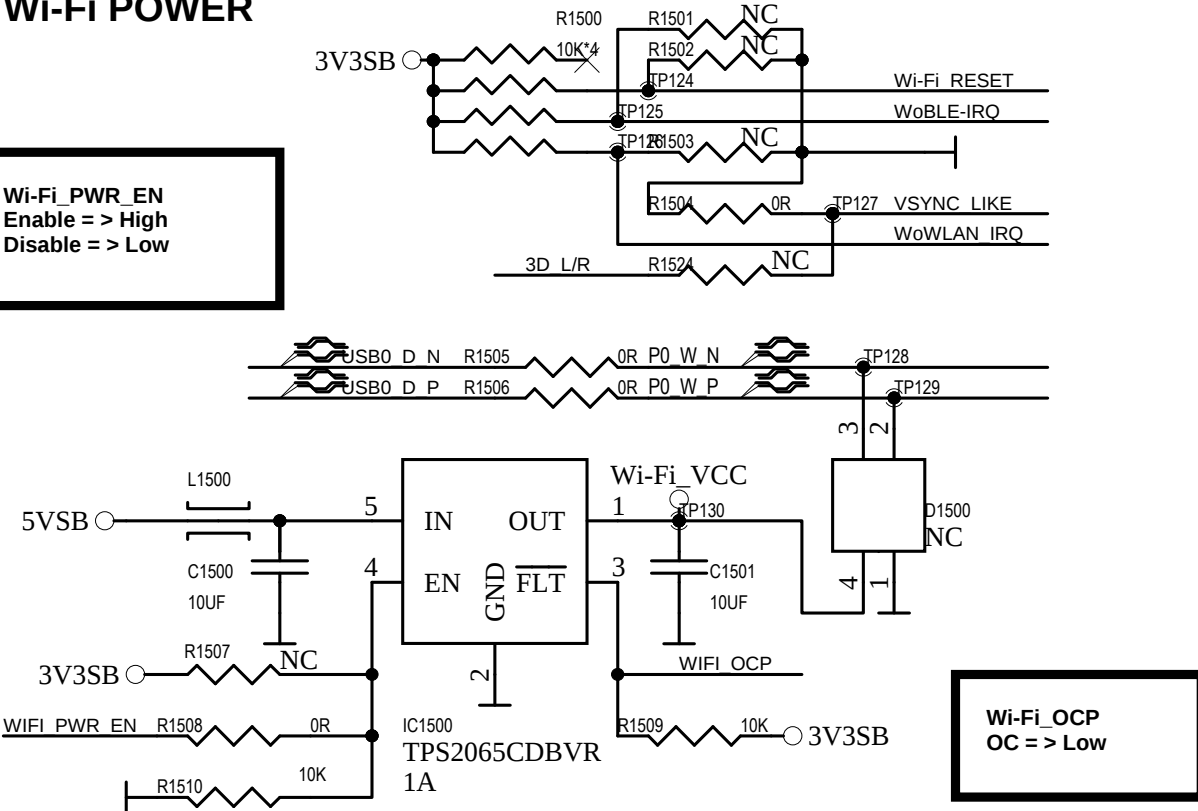


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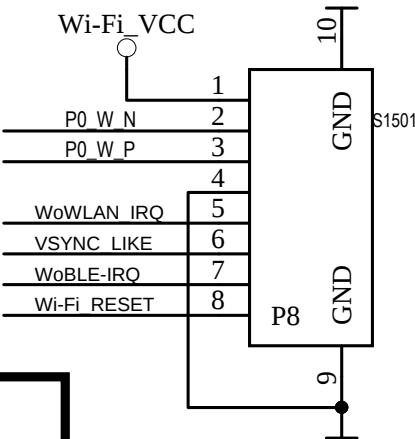


Wi-Fi POWER

Wi-Fi_PWR_EN
Enable => High
Disable => Low



Wi-Fi CONNECTOR



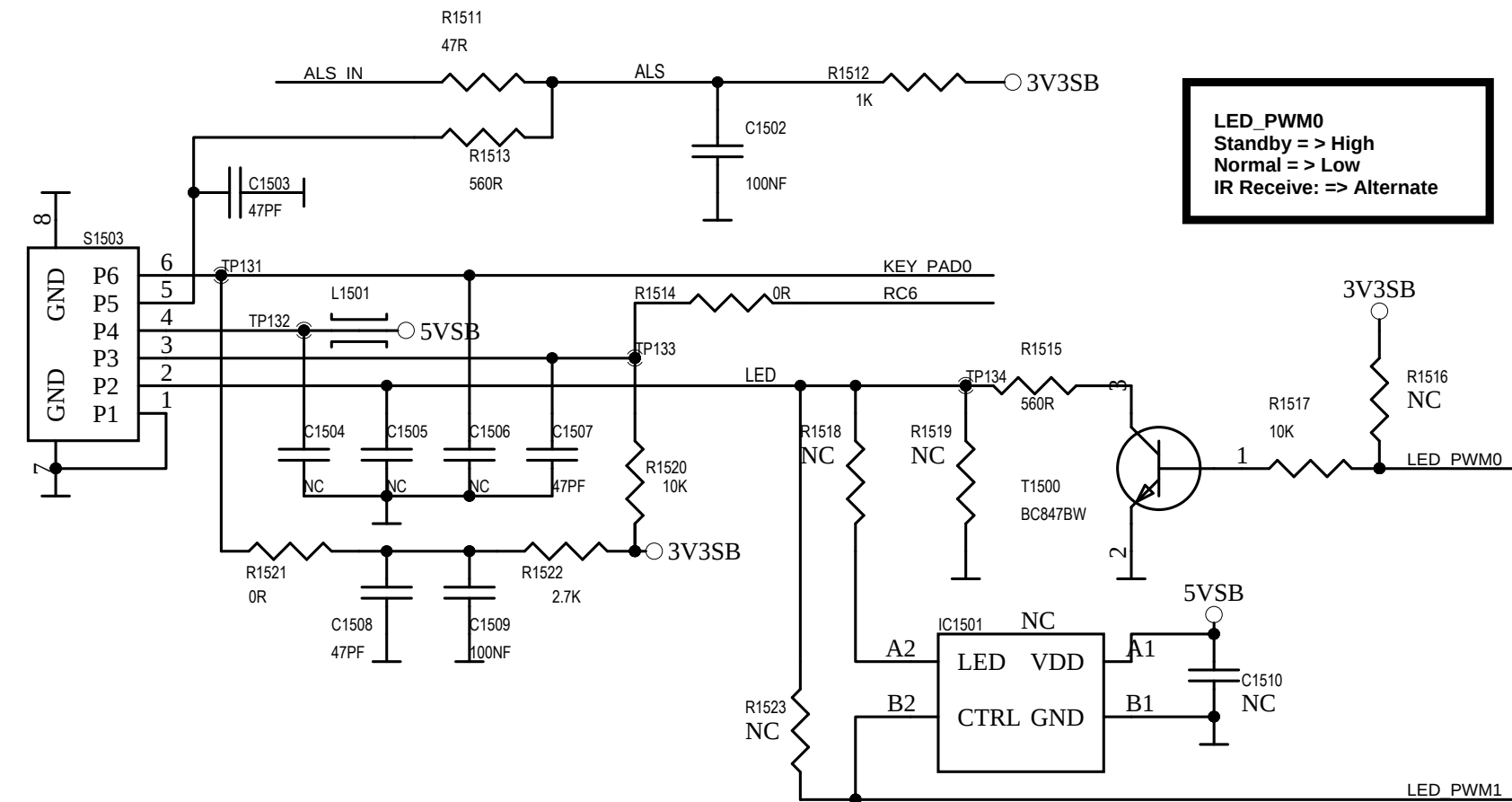
WoBLE-IRQ
Normal => High
Wake event from BT => Low

Wi-Fi_RESET
Normal => High
Reset event from Mai Chip => Low

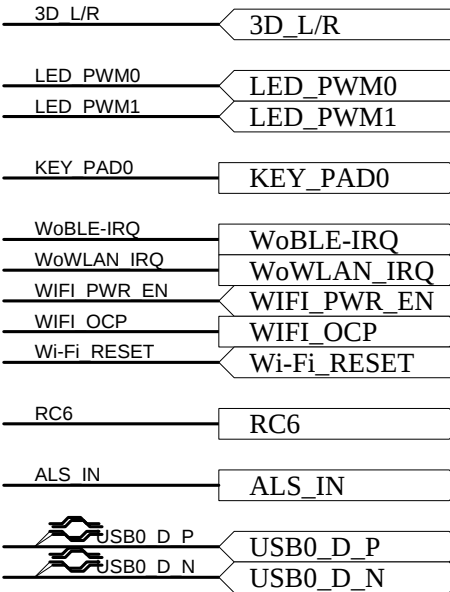
WoWLAN_IRQ
Normal => High
Wake event from Wi-Fi => Low

Wi-Fi_OCP
OC => Low

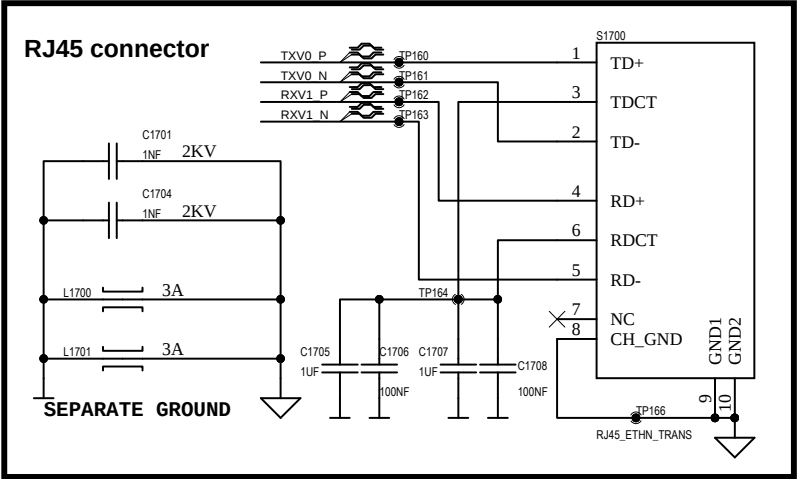
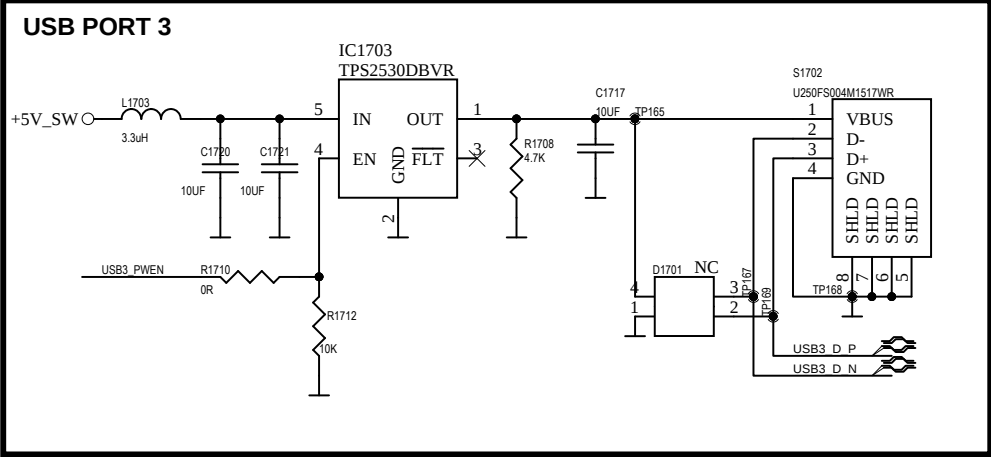
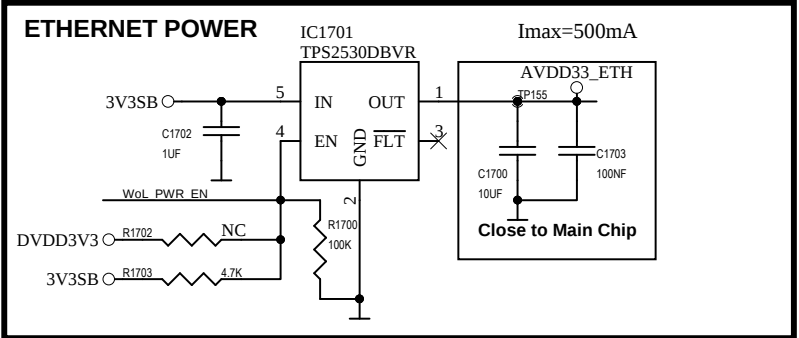
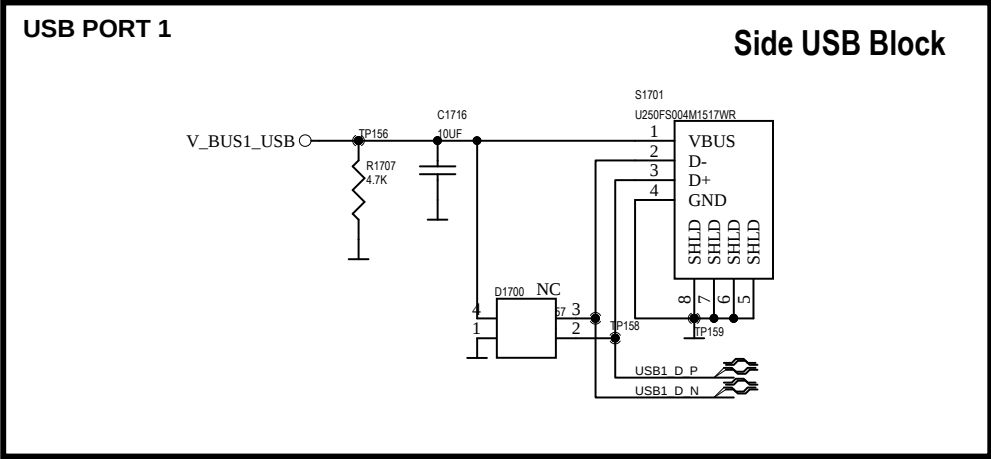
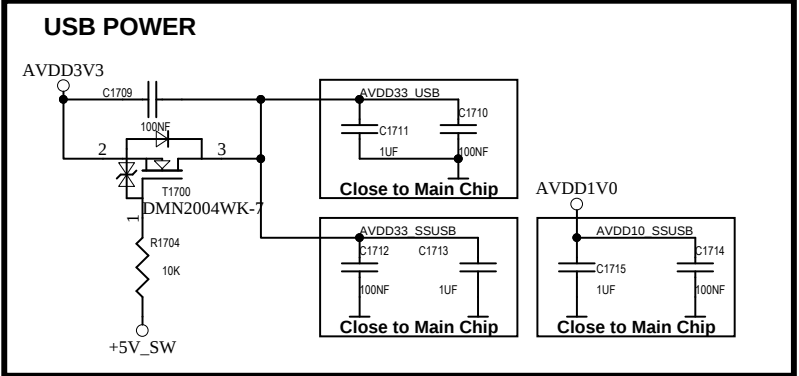
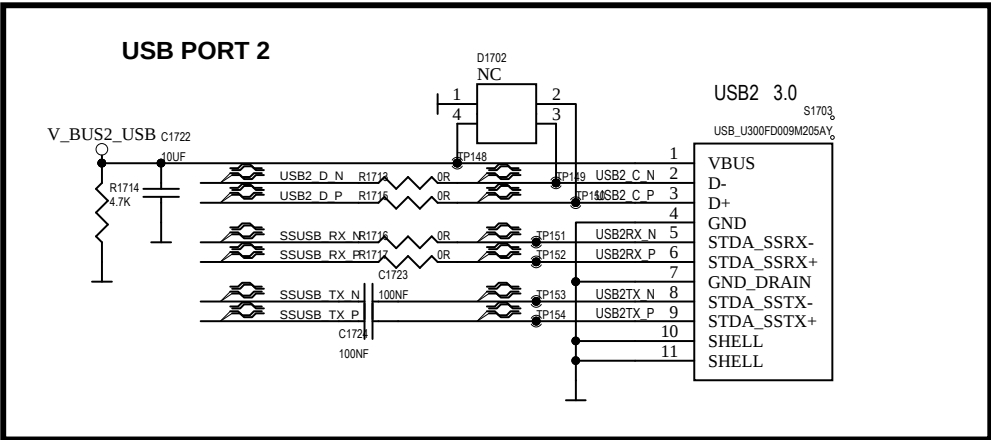
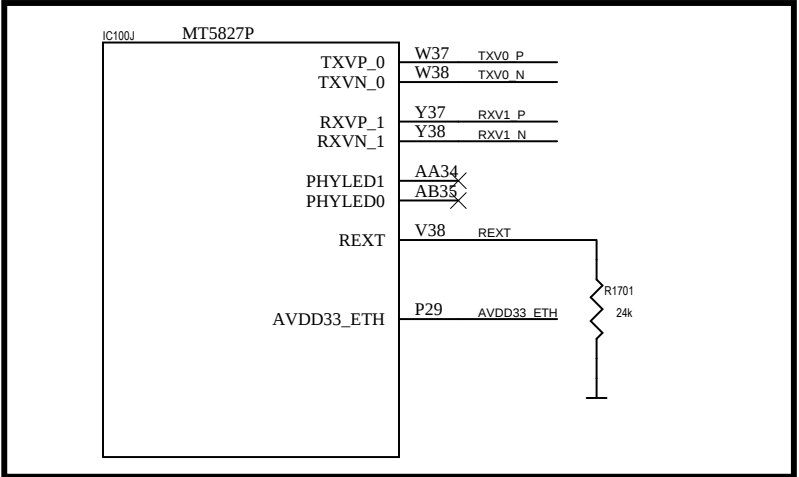
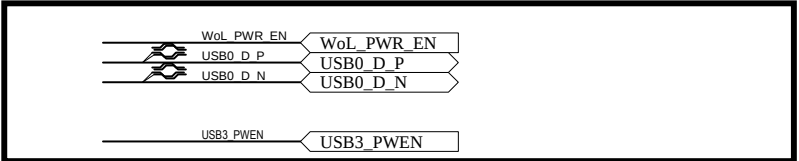
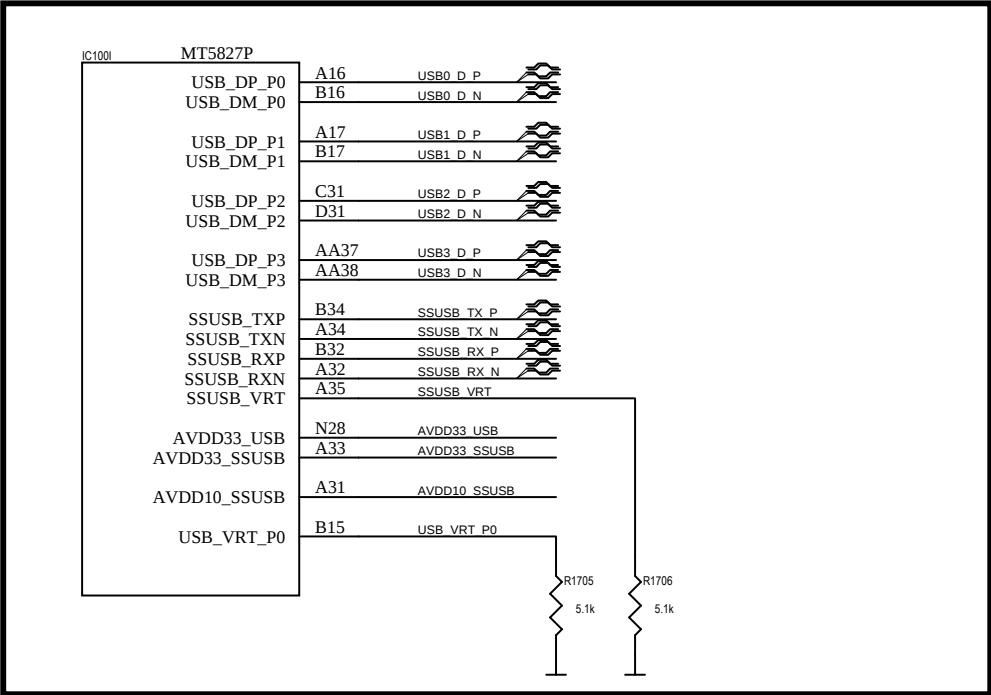
IR/KEY PAD CONNECTOR



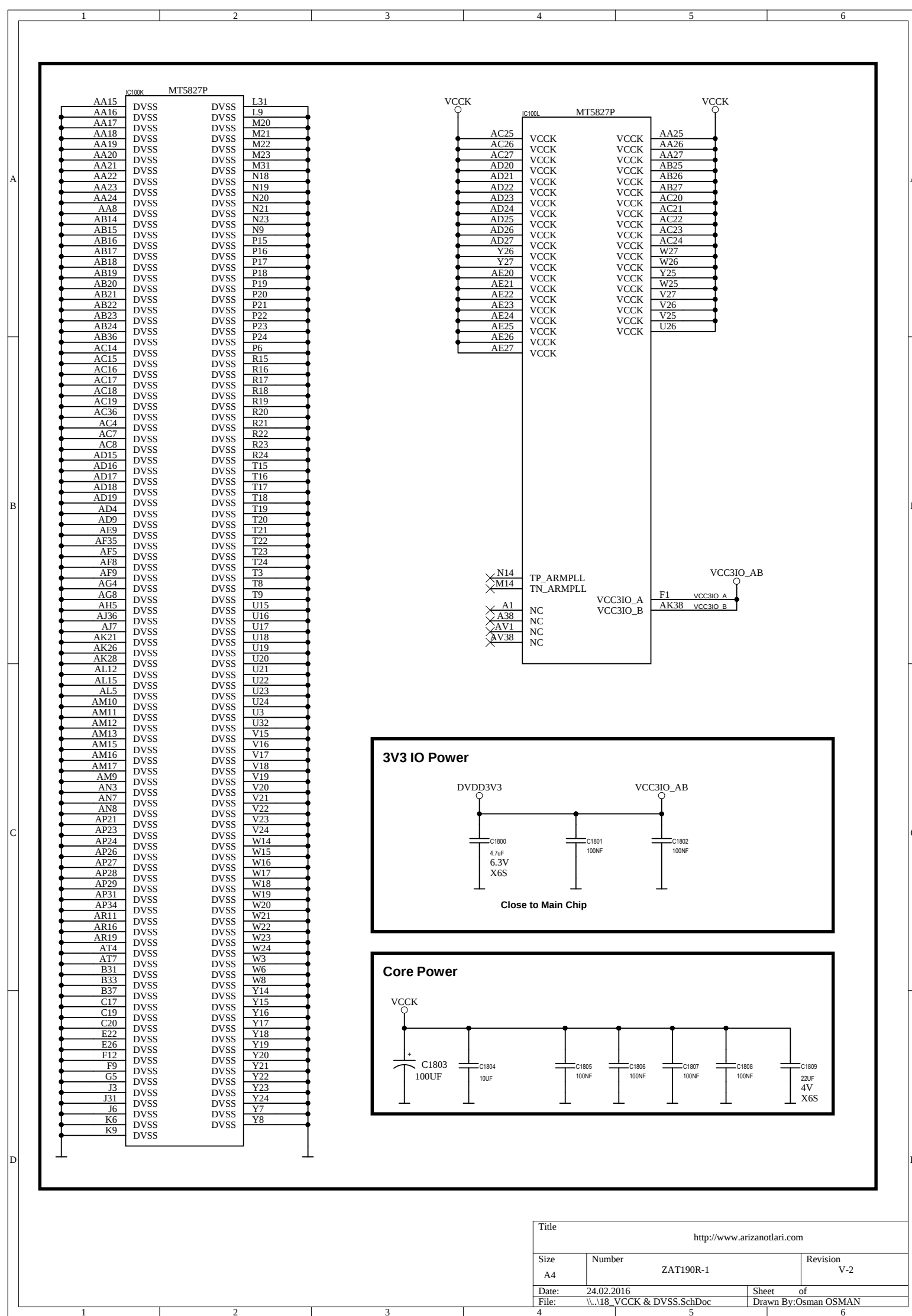
LED_PWM0
Standby => High
Normal => Low
IR Receive: => Alternate

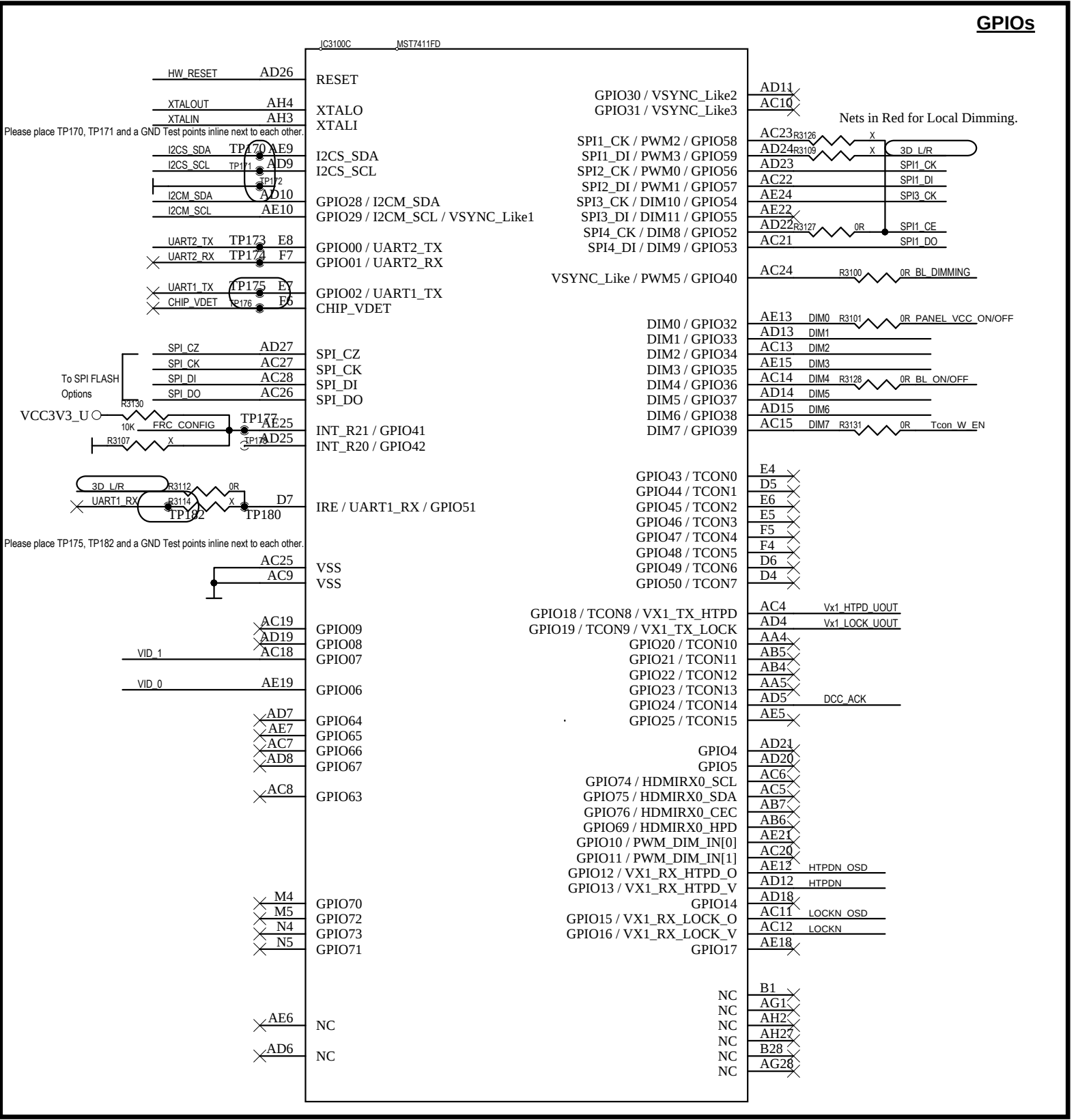
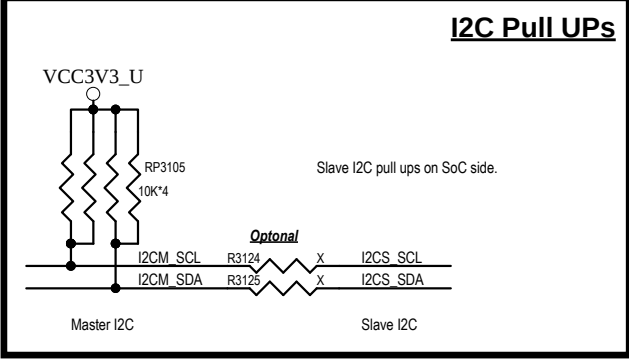
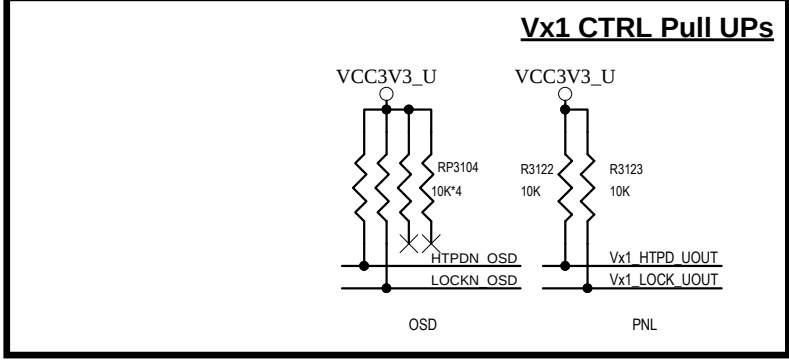
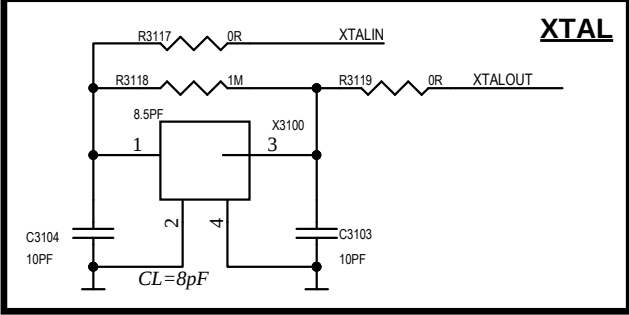
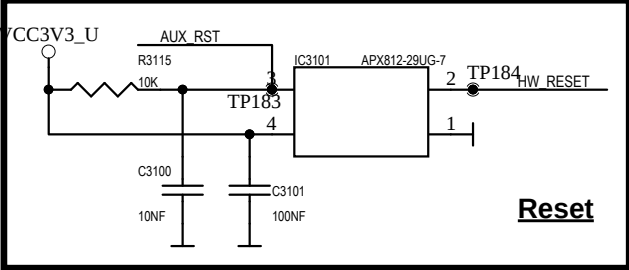
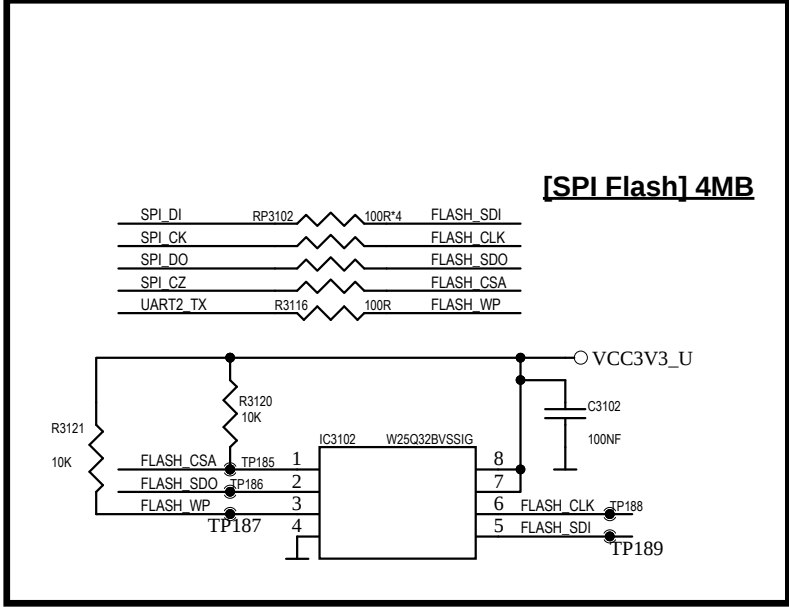
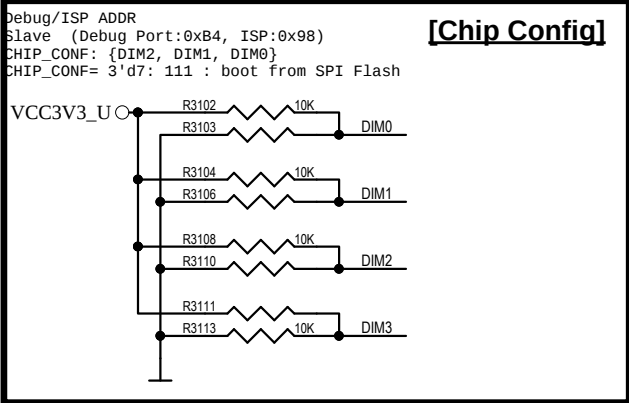
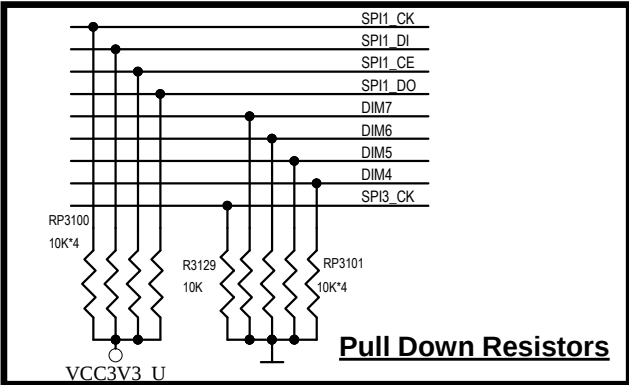
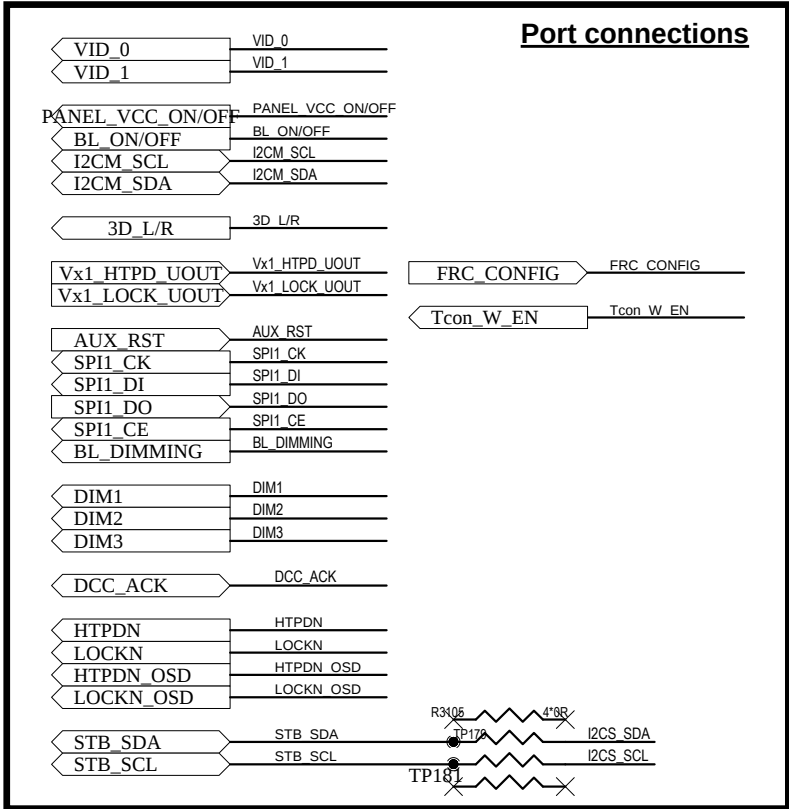


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File:	\\..15_IR_KEYPAD_Wi-Fi_LIGH.SchDoc	Drawn By:		Osman OSMAN	

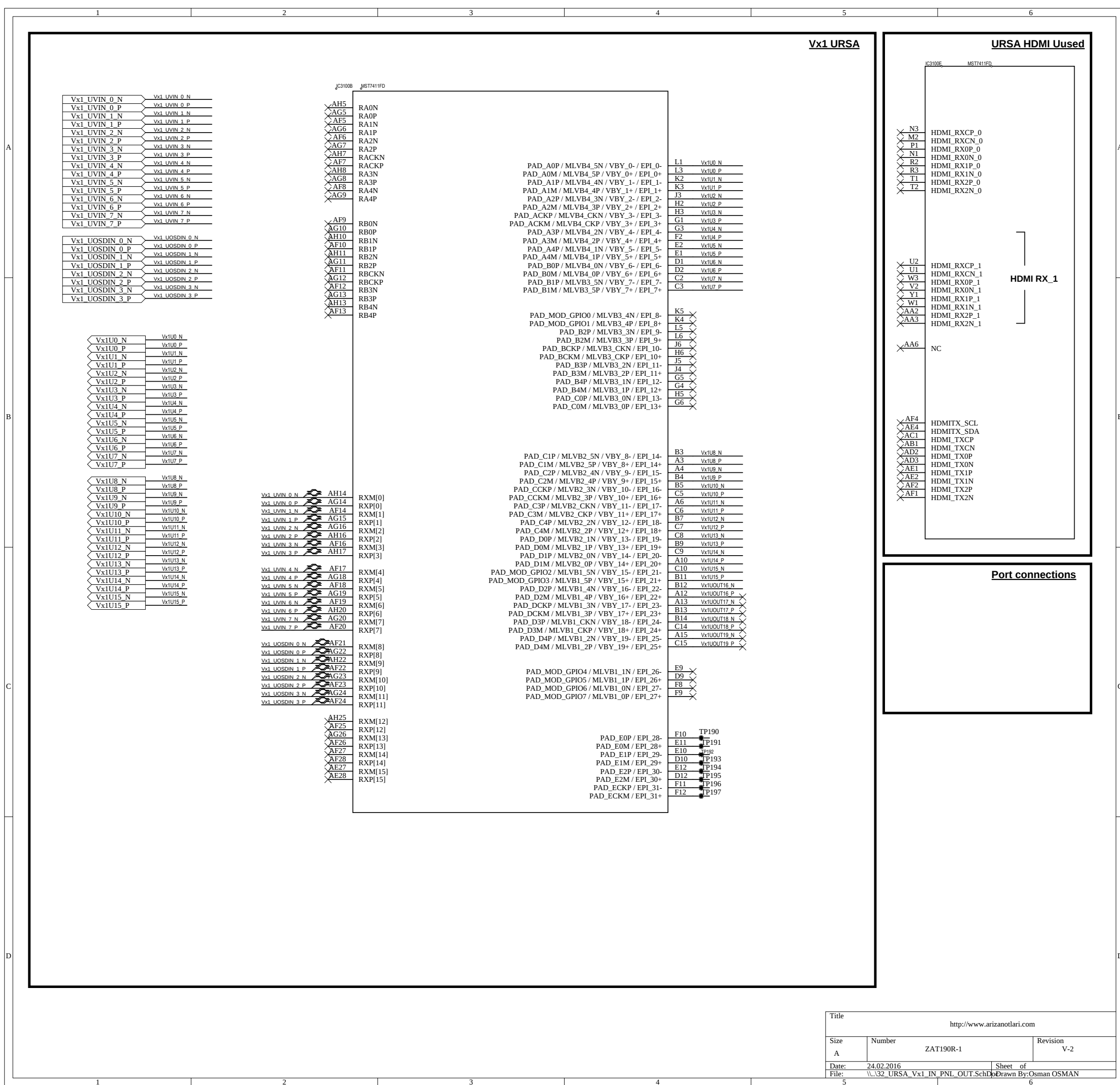


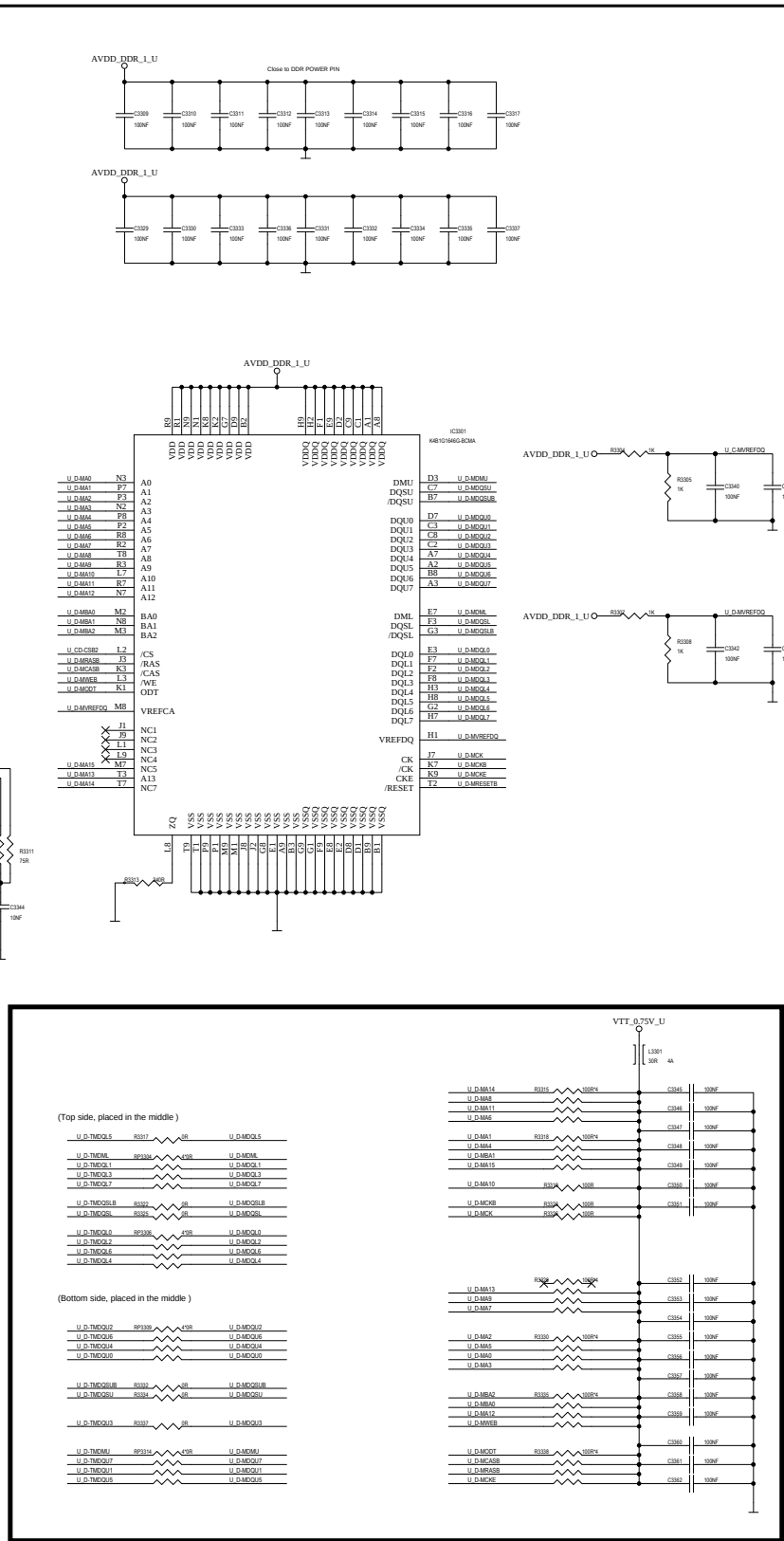
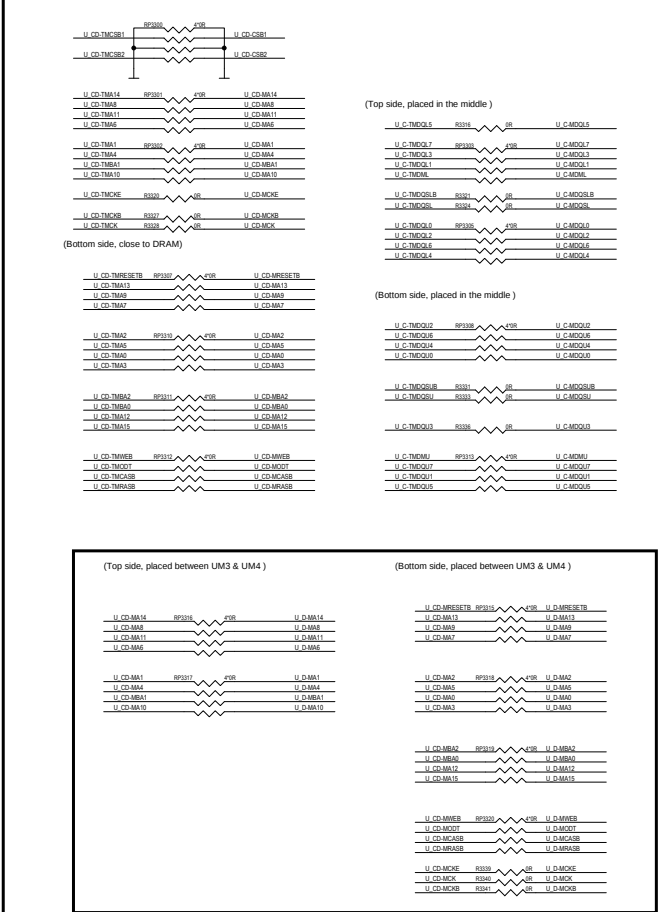
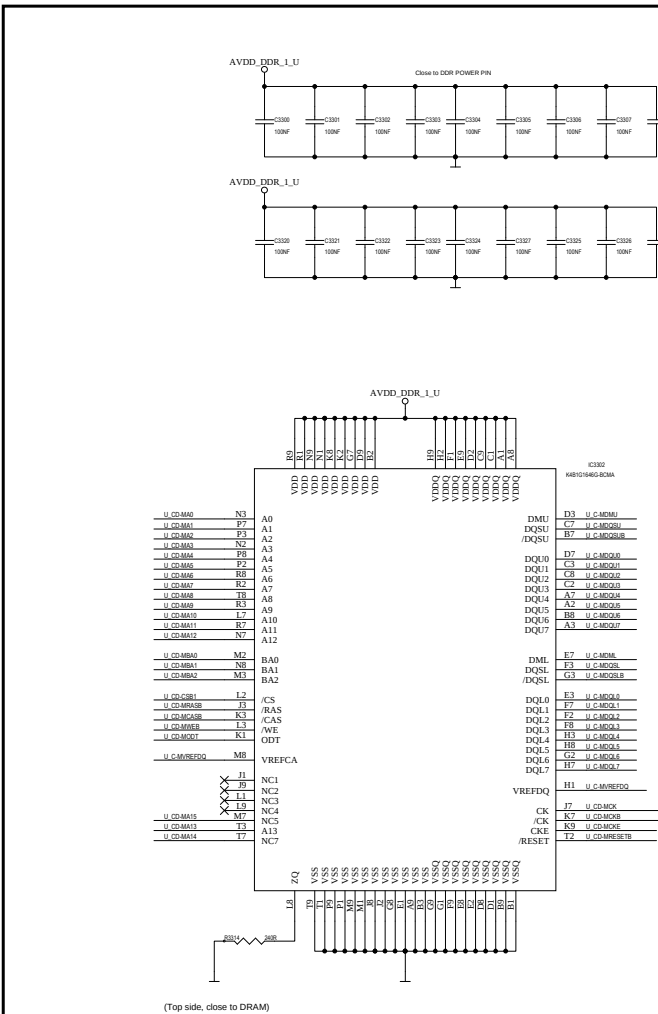
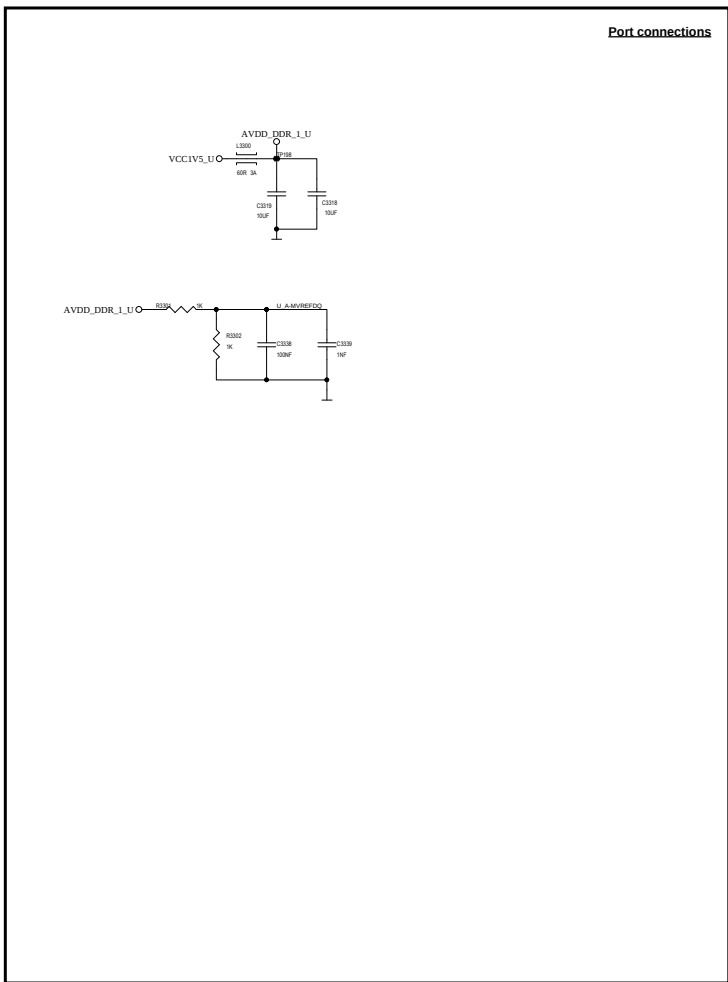
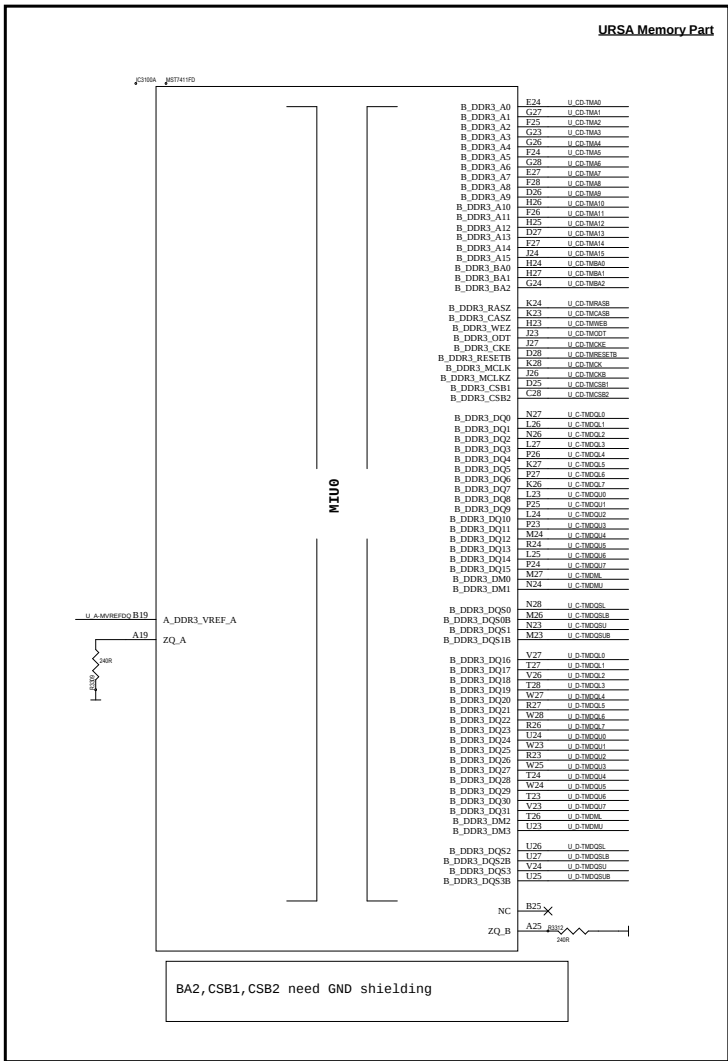
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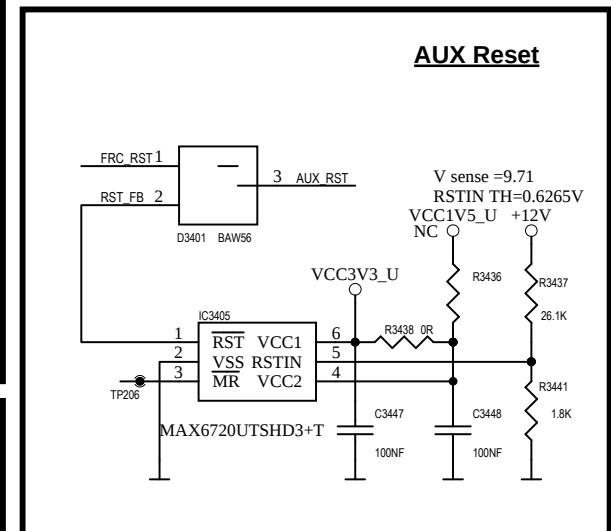
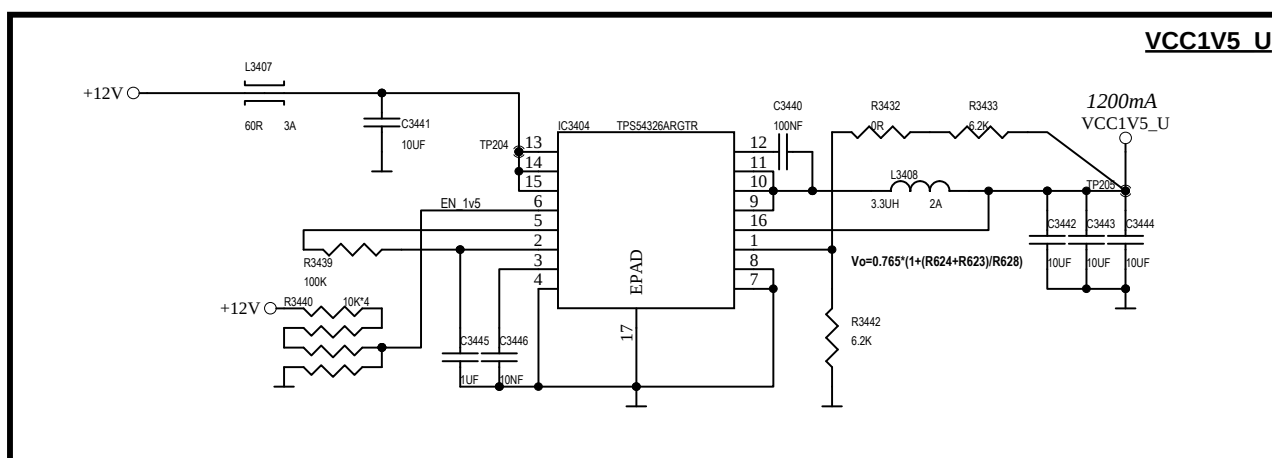
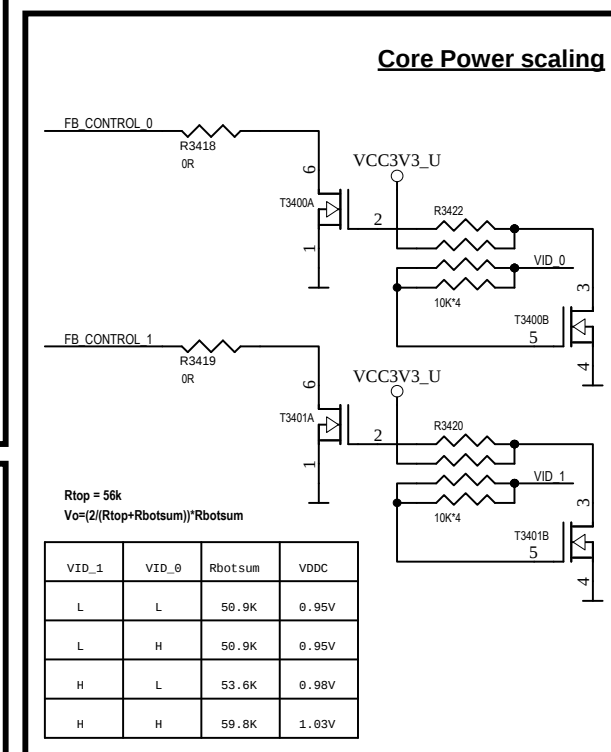
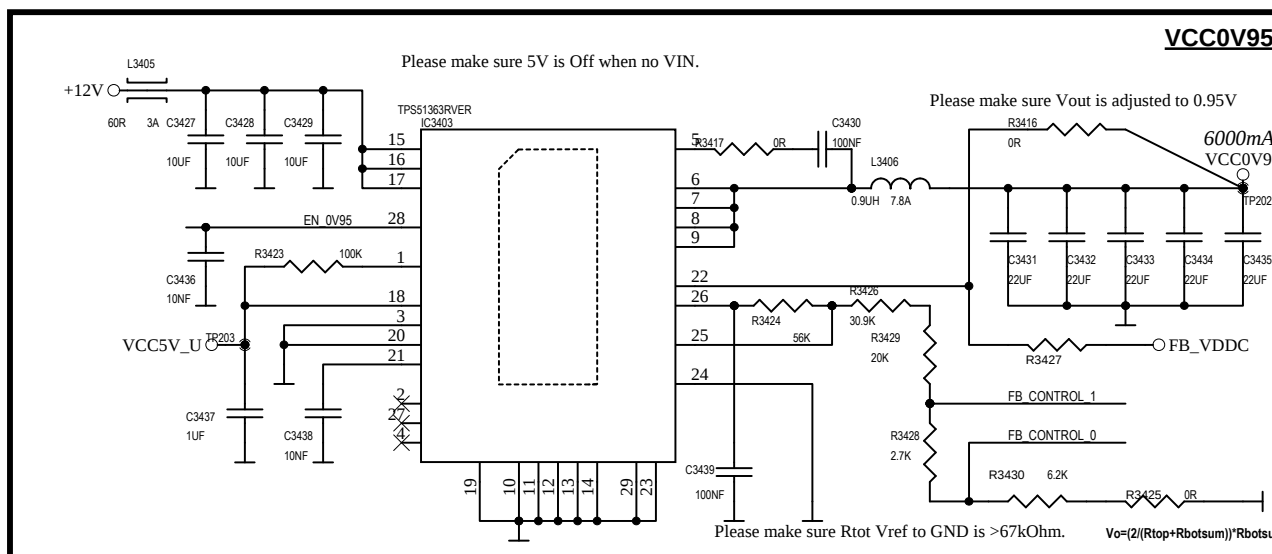
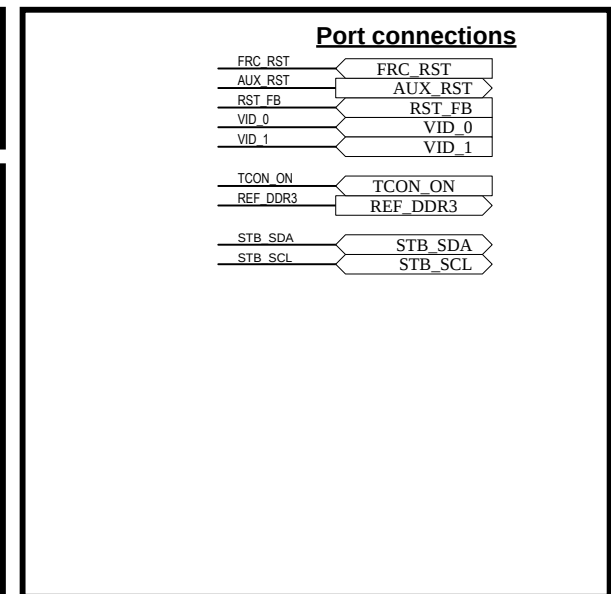
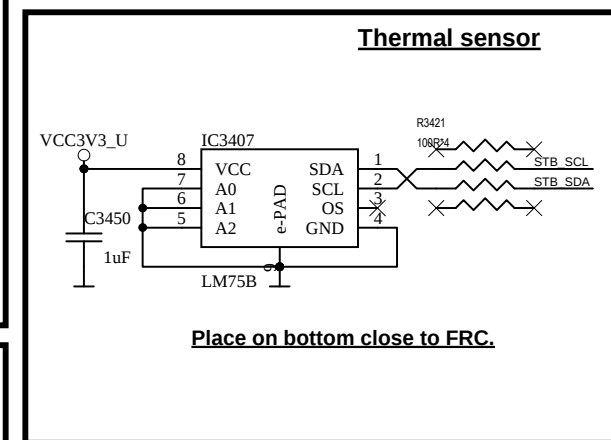
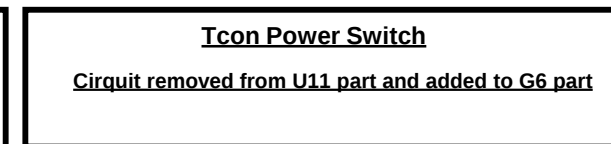
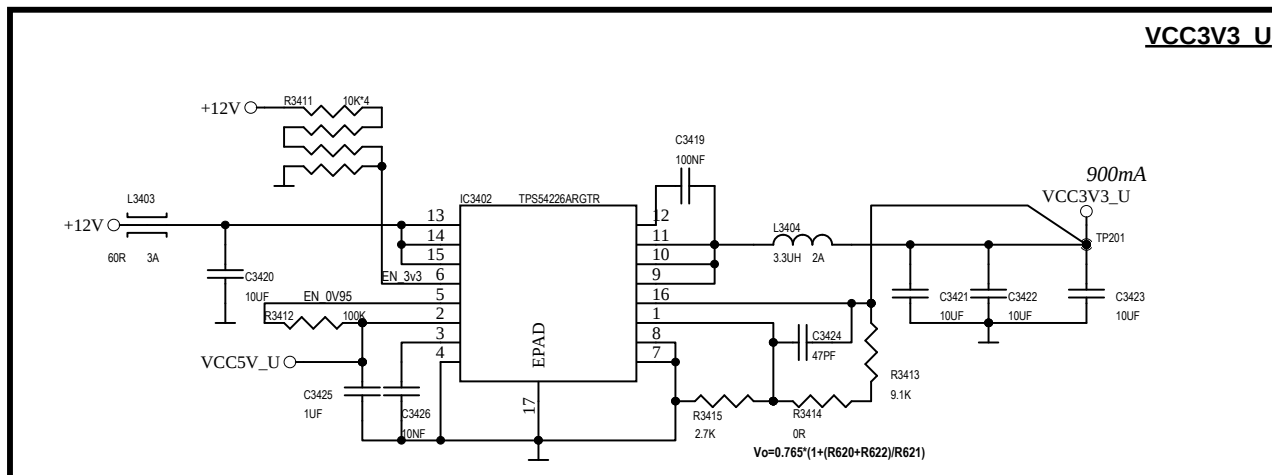
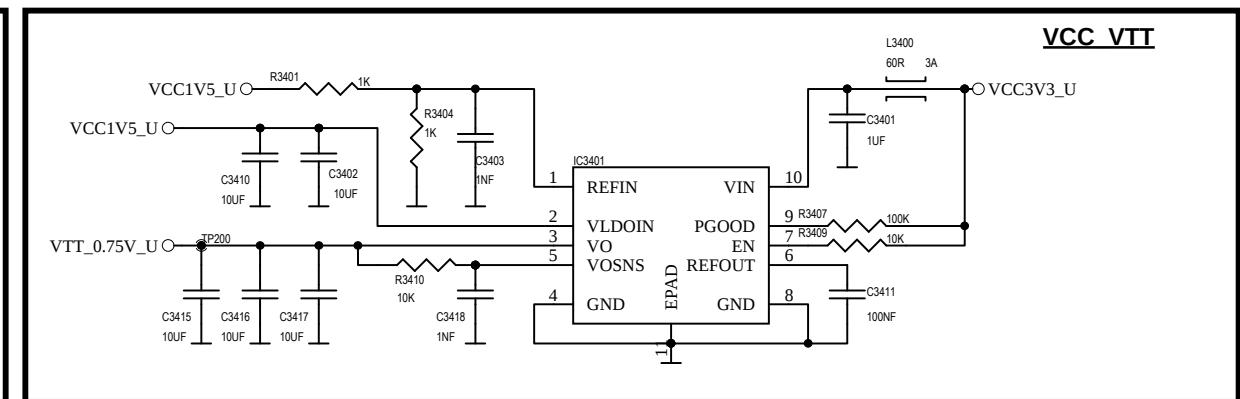
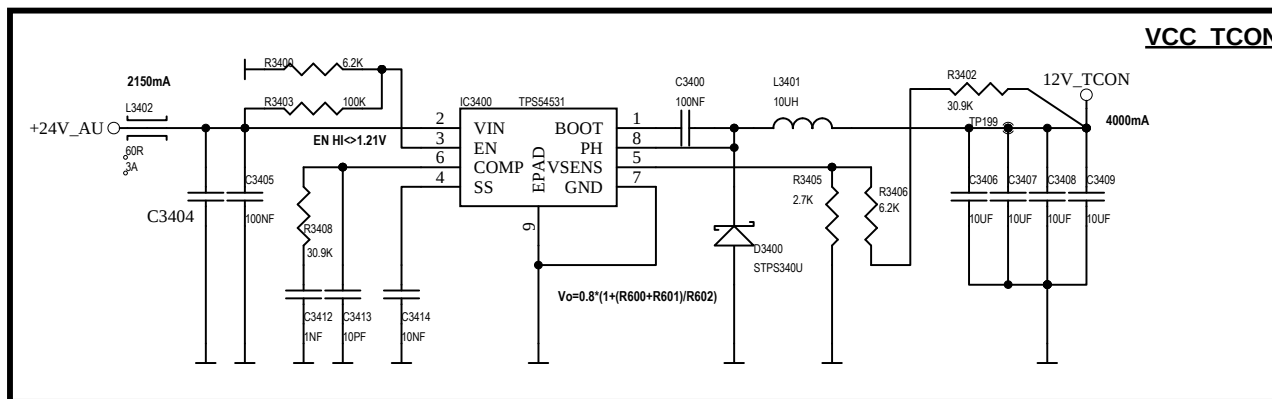


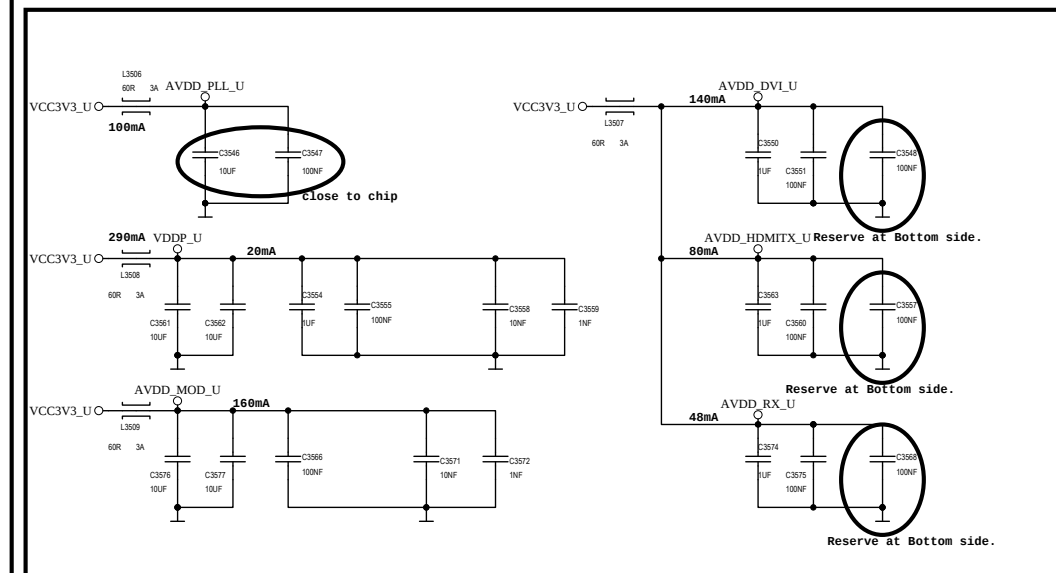
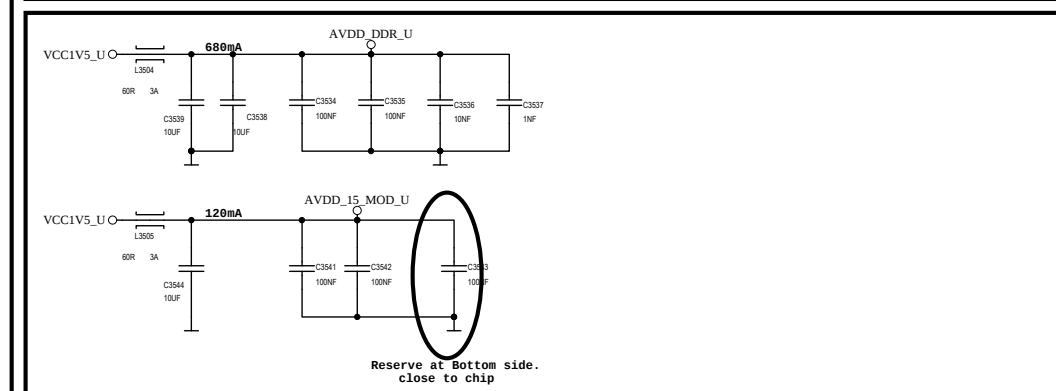
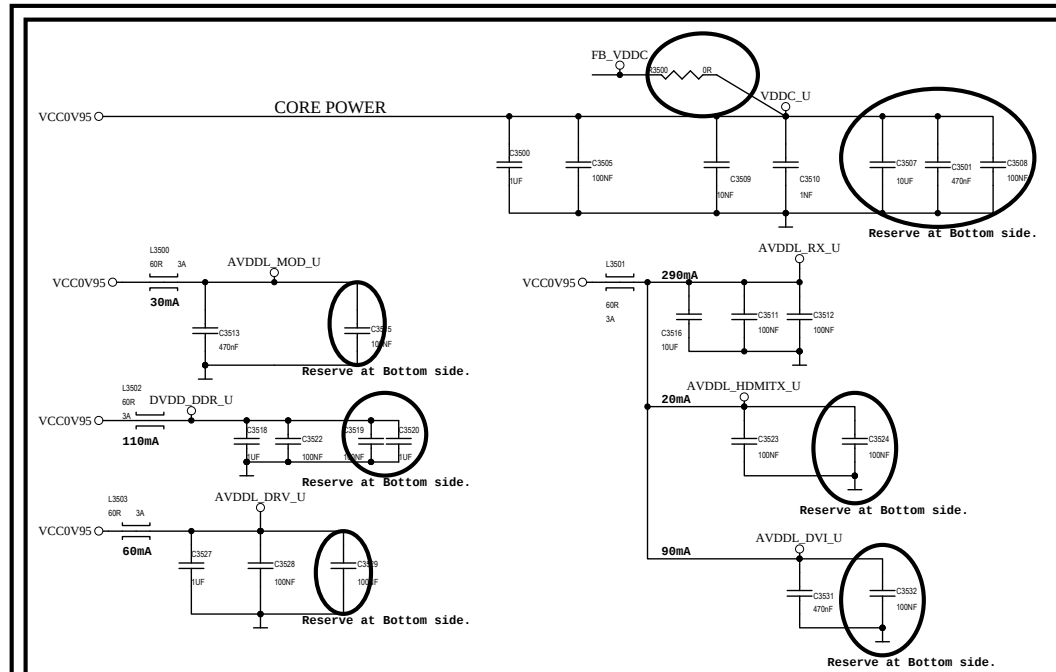


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SoC POWER

